Contents

Features

- ★ PCMCIA / JEIDA standard
- ★ 64K bytes ~ 8M bytes memory capacity
- ★ Byte (x8) / word (x16) data bus selectable
- ★ Fast access time : 150ns (maximum)
- ★ Attribute memory : 2K byte E^2PROM or no attribute memory
- ★ Single +5V operating voltage
- ★ Dual back-up battery design
- ★ Both BR2325 and CR2025 used as main battery
- ★ Battery voltage detection function
- ★ Built-in write protect switch
- ★ Battery case lock system
- ★ Connector type : 2-piece,2-row,68 pins
- ★ Credit card size : 54.0 x 85.6 x 3.3 (mm)
- ★ Commercial / Industrial grade

General Description

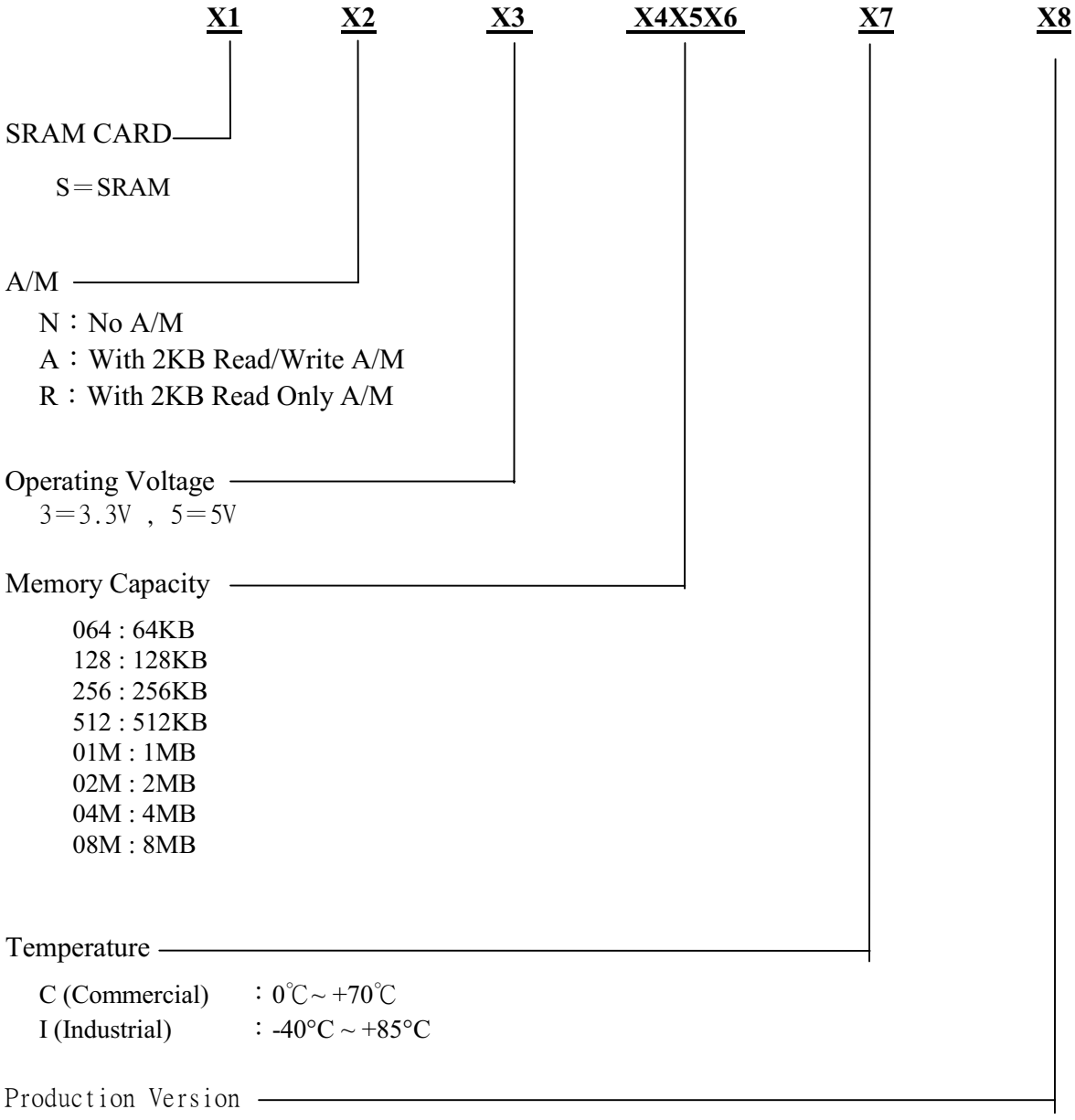
C-ONE's high performance SRAM cards conform to the PCMCIA / JEIDA international standard and consist of multiple very low power consumption CMOS SRAM ICs , decoder IC and power control IC mounted on a very thin printed circuit board using surface mounting technology.

With the dual back-up battery design , each SRAM card contains a replaceable but non-rechargeable 3V lithium battery (main battery) and an on-board rechargeable but non-replaceable battery (auxiliary battery) for data retention. This design allows replacement of main battery without data loss for 20 minutes approximately. Digital signals on the BVD1*/BVD2* pins were used to alarm the user whether the main battery should be replaced to prevent the stored data from loss. With the flexible and user-friendly design , both BR2325 and CR2025 can be used as main battery. There is battery case lock system to prevent battery dropping from the card. Also , with the write-protect switch design , data will not be written into the card by accident.

Memory card attribute information represents various attribute information of a card and is stored at EVEN address of an attribute memory space which is enabled by asserting REG* signal. Regarding to the attribute information format , please refer to the PCMCIA 2.0 or JEIDA 4.1 specification.

With the flexible design of this series cards , they provide 2K bytes E^2PROM available for attribute memory or there is no attribute memory.

Product Number Definition



Note : A/M means attribute memory.

Product List

(Commercial grade)

Item No.	Part Number	Memory Capacity		Attribute Memory	Power Consumption
		Bytes	Words		
1	SA5064C	64K	32K	2KB E^2PROM	Super Low
2	SA5128C	128K	64K		
3	SA5256C	256K	128K		
4	SA5512C	512K	256K		
5	SA501MC	1M	512K		
6	SA502MC	2M	1M		
7	SA504MC	4M	2M		
8	SA508MC	8M	4M		
9	SN5064C	64K	32K	None	
10	SN5128C	128K	64K		
11	SN5256C	256K	128K		
12	SN5512C	512K	256K		
13	SN501MC	1M	512K		
14	SN502MC	2M	1M		
15	SN504MC	4M	2M		
16	SN508MC	8M	4M		

(Industrial grade)

Item No.	Part Number	Memory Capacity		Attribute Memory	Power Consumption
		Bytes	Words		
1	SA5064I	64K	32K	2KB E^2PROM	Super Low
2	SA5128I	128K	64K		
3	SA5256I	256K	128K		
4	SA5512I	512K	256K		
5	SA501MI	1M	512K		
6	SA502MI	2M	1M		
7	SA504MI	4M	2M		
8	SA508MI	8M	4M		
9	SN5064I	64K	32K	None	
10	SN5128I	128K	64K		
11	SN5256I	256K	128K		
12	SN5512I	512K	256K		
13	SN501MI	1M	512K		
14	SN502MI	2M	1M		
15	SN504MI	4M	2M		
16	SN508MI	8M	4M		

Table 1

Pin Configuration

(SA508MC , SA508MI series)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Pin No.
VCC	BUSY*	WE*	A14	A13	A8	A9	A11	OE*	A10	CE1*	D7	D6	D5	D4	D3	GND	Pin Name
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	Pin No.
GND	WP	D2	D1	D0	A0	A1	A2	A3	A4	A5	A6	A7	A12	A15	A16	NC	Pin Name
51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	Pin No.
VCC	A21	A20	A19	A18	A17	NC	NC	NC	CE2*	D15	D14	D13	D12	D11	CD1*	GND	Pin Name
68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	Pin No.
GND	CD2*	D10	D9	D8	BVD1*	BVD2*	REG*	NC	NC	NC	NC	NC	NC	NC	A22	NC	Pin Name

Table 2

Note : * mean low active

64KB series : A16,A17,A18,A19,A20,A21,A22 = NC

128KB series : A17,A18,A19,A20,A21,A22 = NC

256KB series : A18,A19,A20,A21,A22 = NC

512KB series : A19,A20,A21,A22 = NC

1MB series : A20,A21,A22 = NC

2MB series : A21,A22 = NC

4MB series : A22 = NC

SA5064x ~ SA508Mx (x = C, I) series : pin16 = BUSY* , pin61 = REG*

SN5064x ~ SN508Mx (x = C, I) series : pin16 = NC , pin61 = NC

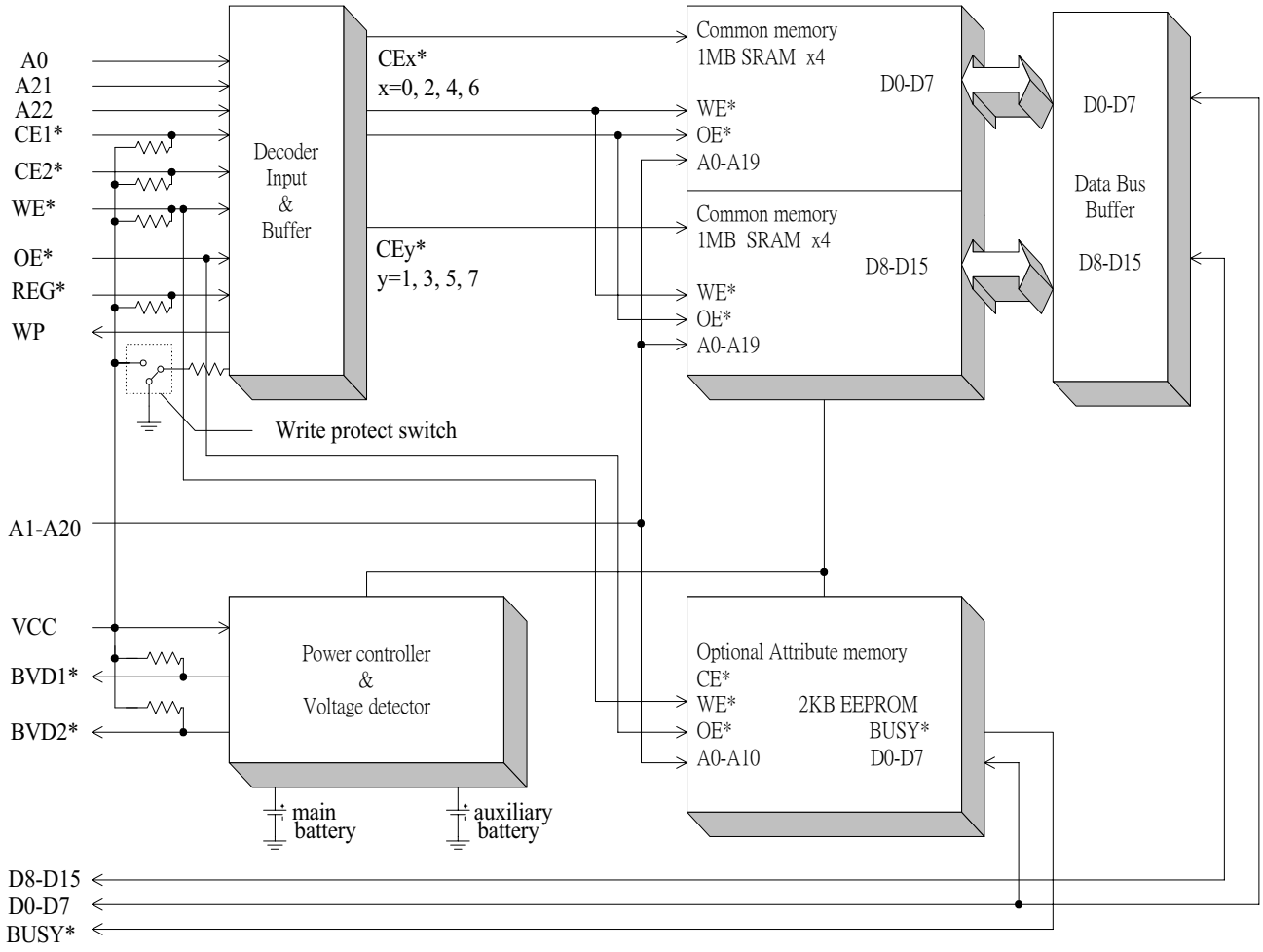
Pin Description

Symbol	Function	I/O
A0 - A22	Addresses	I
D0 - D15	Data Inputs/Outputs	I/O
CE1*/CE2*	Card Enable	I
OE*	Output Enable	I
WE*	Write Enable	I
REG*	Attribute Memory Enable	I
WP	Write-protect Detect	O
BVD1*/BVD2*	Battery Voltage Detect	O
BUSY*	Busy Output (Open drain)	O
CD1*/CD2*	Card Detect (tied to GND internally)	O
VCC	+5 Volt Power Supply	-
GND	Ground	-
NC	No Connection	-

Table 3

Block Diagram

(8MB series SRAM card)

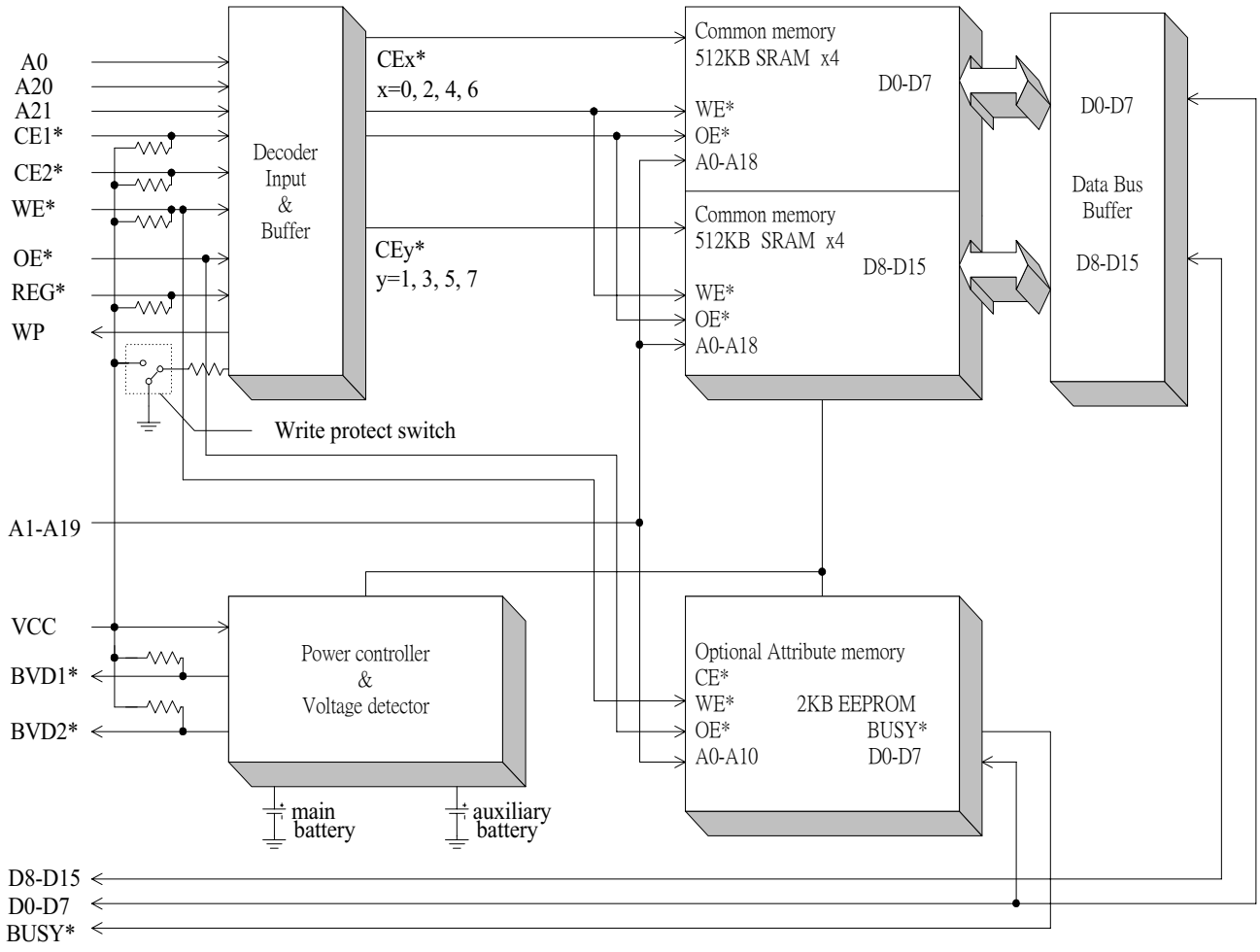


Note : A0,A21,A22 are chip decoding address pins.

Figure 1

Block Diagram

(4MB series SRAM card)

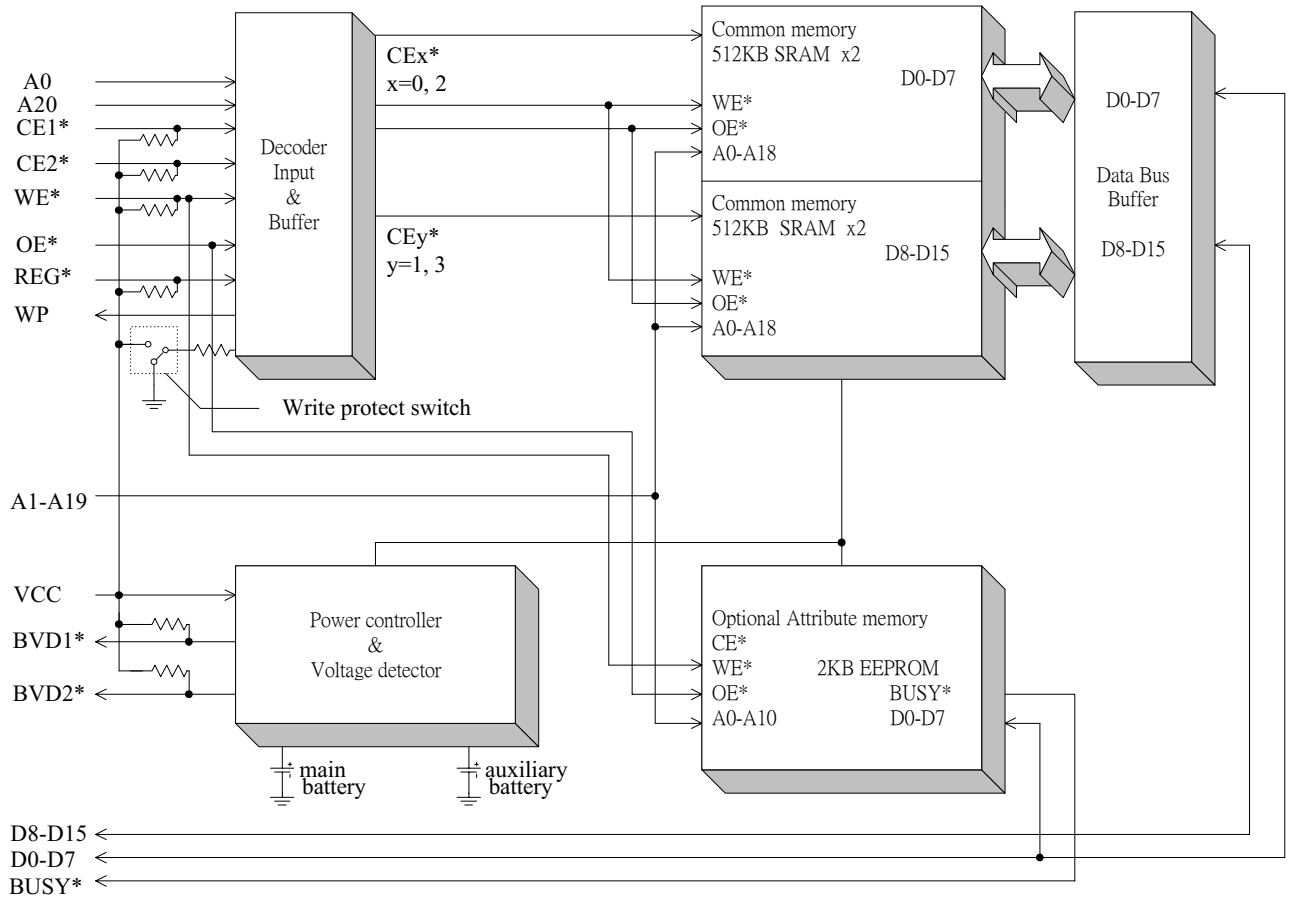


Note : A0,A20,A21 are chip decoding address pins.

Figure 2

Block Diagram

(2MB series SRAM card)

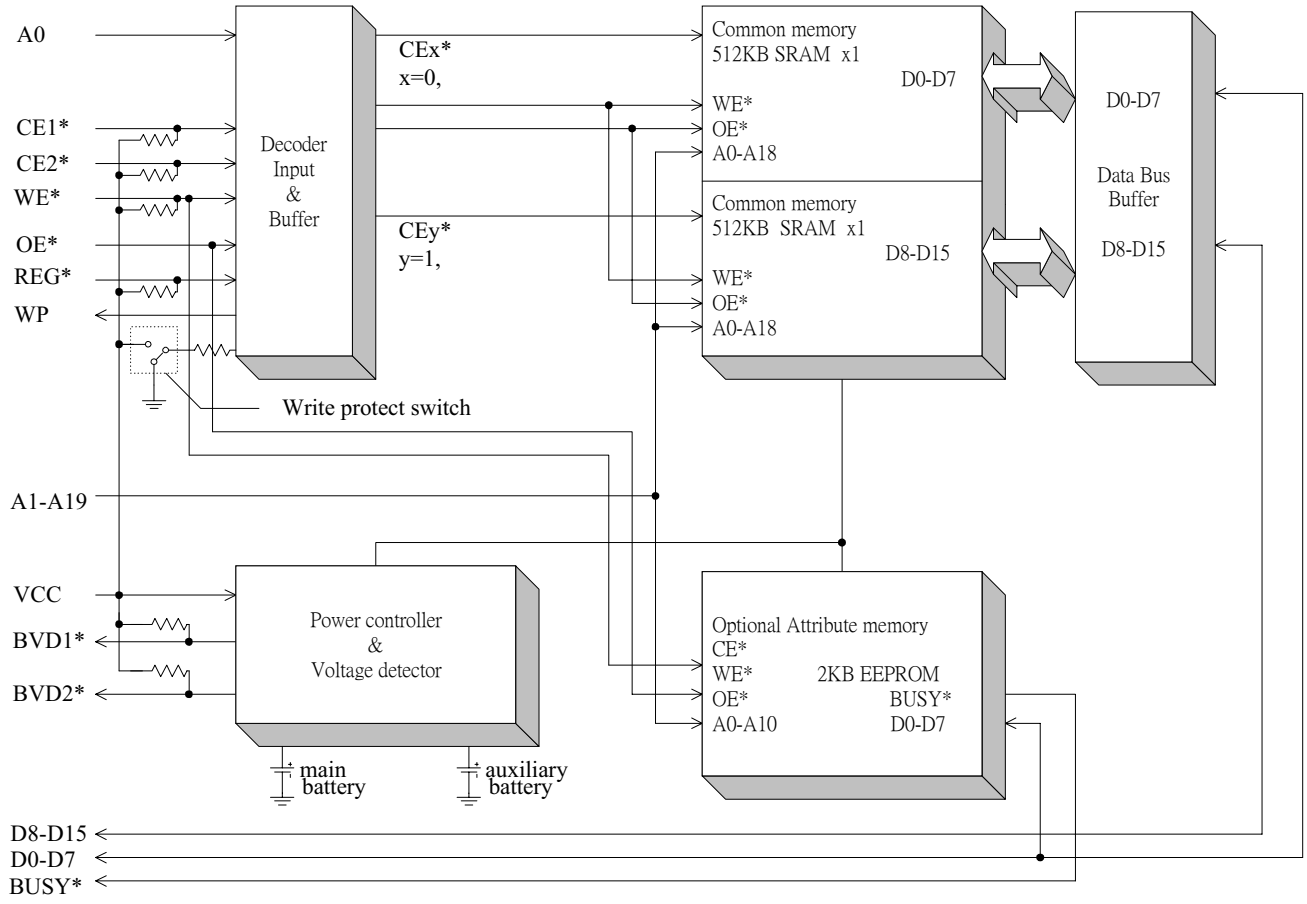


Note : A0,A20 are chip decoding address pins.

Figure 3

Block Diagram

(1MB series SRAM card)

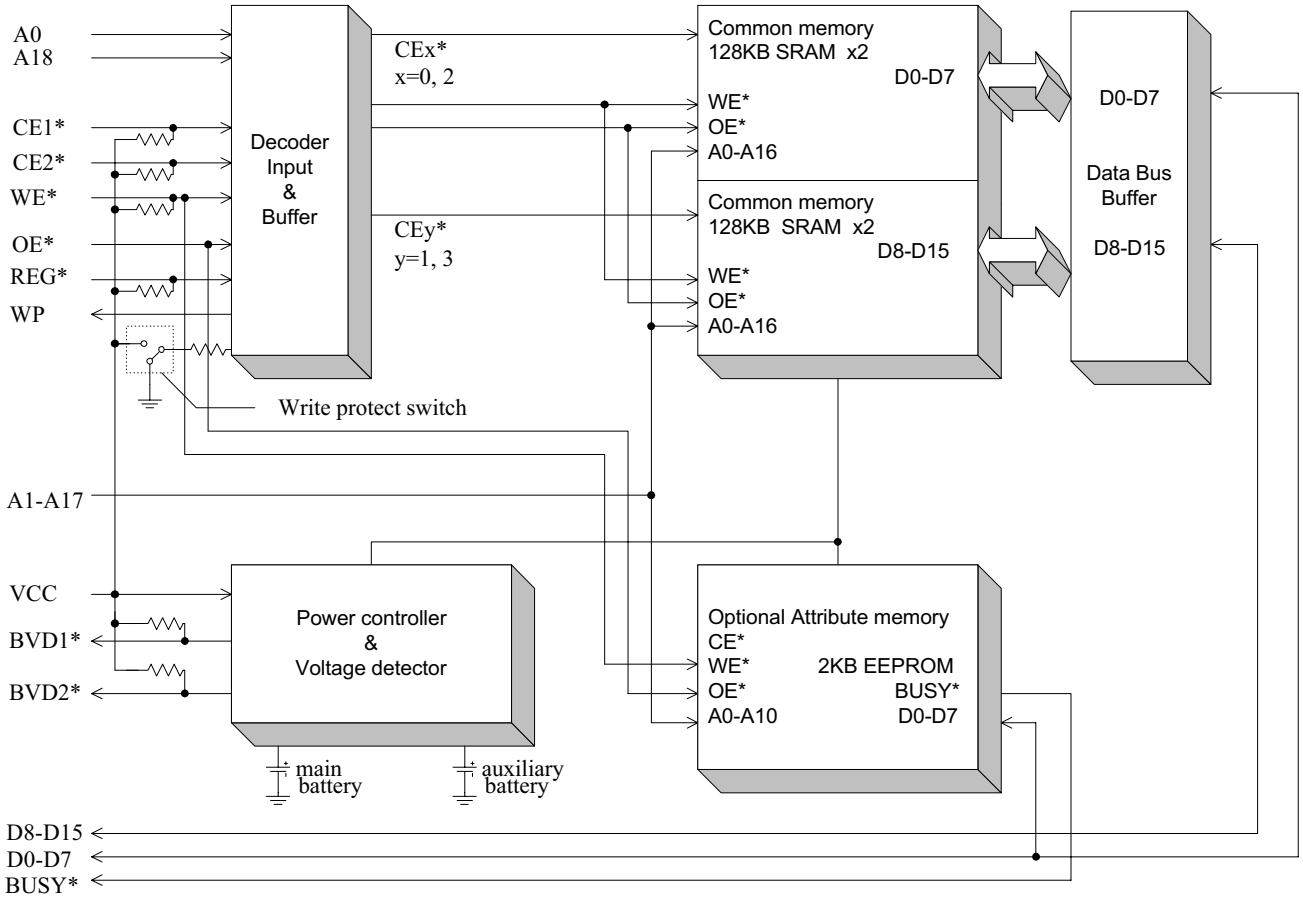


Note : A0 is chip decoding address pin.

Figure 4

Block Diagram

(512KB series SRAM card)

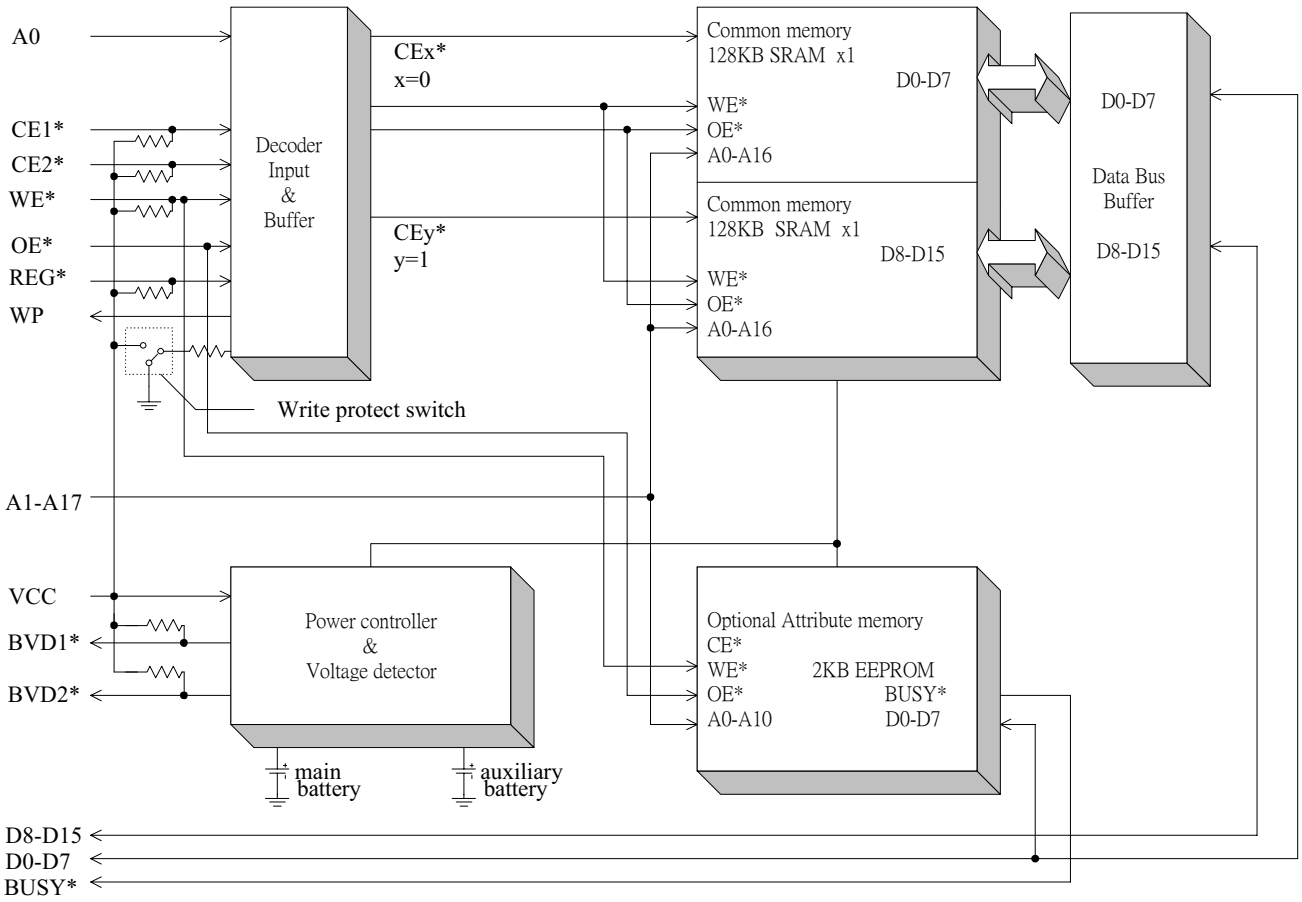


Note : A0,A18 are chip decoding address pins.

Figure 5

Block Diagram

(256KB series SRAM card)

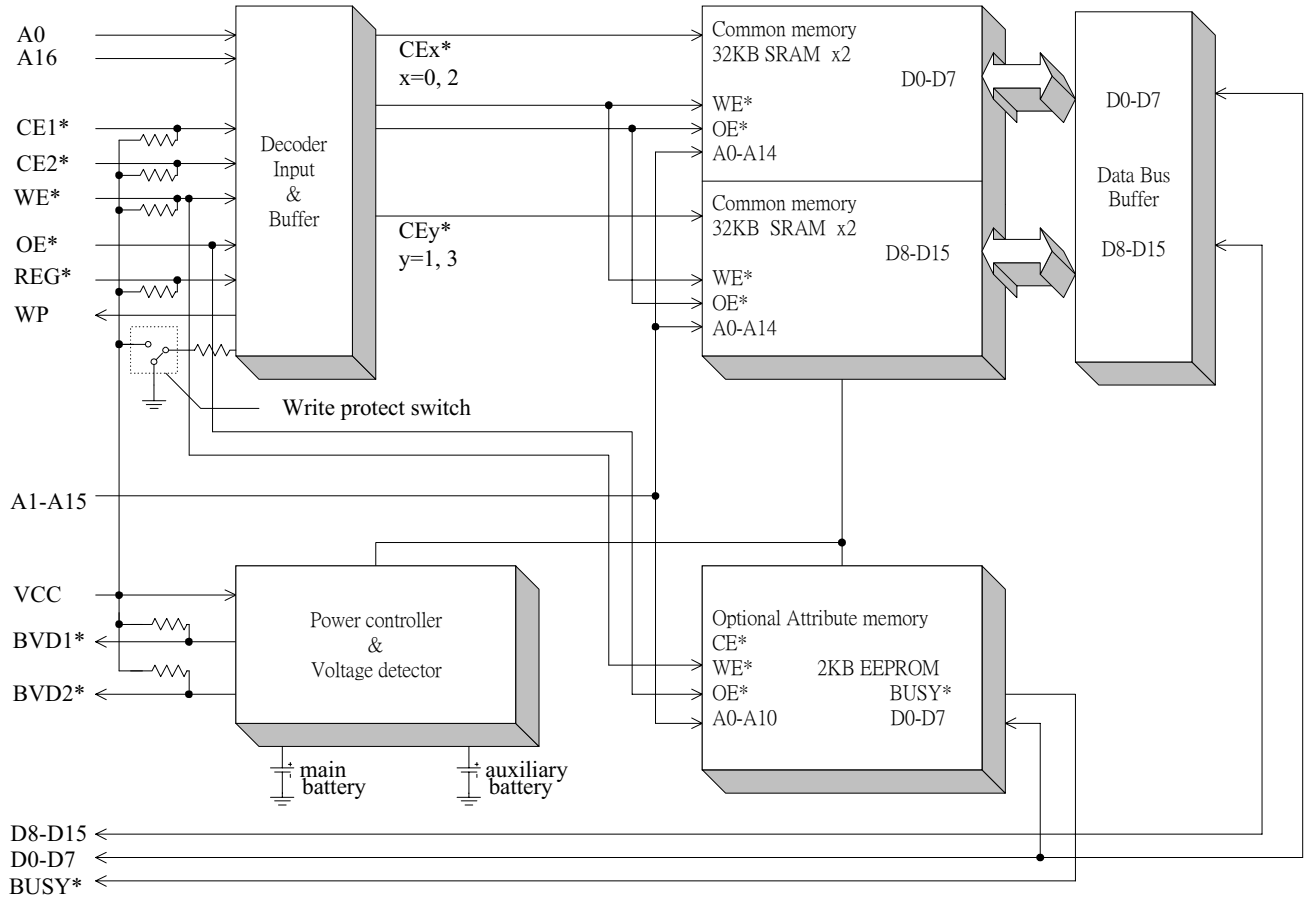


Note : A0 is chip decoding address pin.

Figure 6

Block Diagram

(128KB series SRAM card)

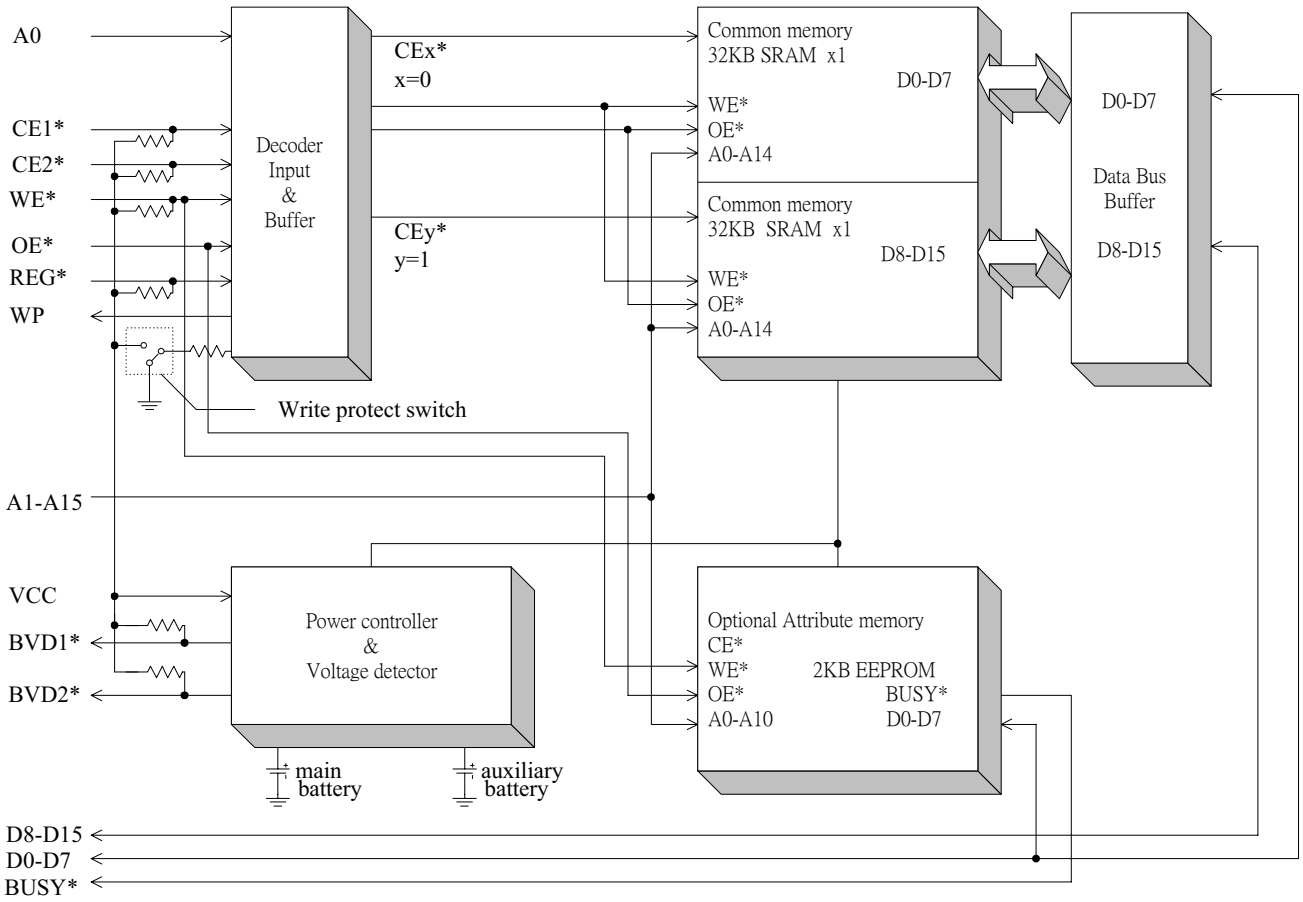


Note : A0,A16 are chip decoding address pins.

Figure 7

Block Diagram

(64KB series SRAM card)



Note : A0 is chip decoding address pin.

Figure 8

Pin Location

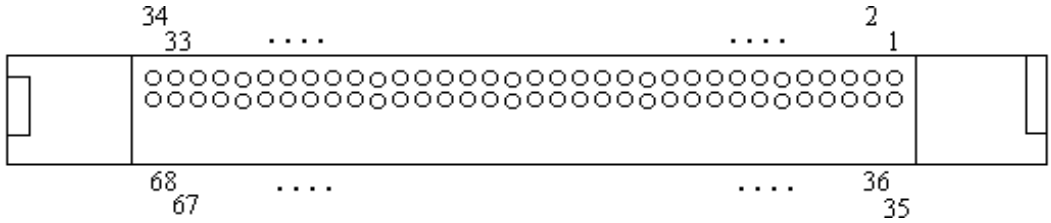


Figure 9 Bottom View (Connector Side)

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	0.7VCC	VCC + 0.3	V
Input Low Voltage	V_{IL}	- 0.3	0.8	V
Battery Voltage	V_{BAT}	2.37		V
Operating Temperature (Commercial)	T_{OPR}	0	60	℃
Operating Temperature (Industrial)	T_{OPR}	-40	85	℃
Relative Humidity (non-condensing)	H_{UM}		95	%

Table 4

Absolute Maximum Ratings *

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to + 6.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC} + 0.3 (6V max.)	V
Output Voltage	V_{OUT}	-0.5 to + 6.0	V
Operating Temperature (Commercial)	T_{OPR}	-10 to + 70	℃
Storage Temperature (Commercial)	T_{STR}	-20 to + 70	℃
Operating Temperature (Industrial)	T_{OPR}	-40 to + 85	℃
Storage Temperature(Industrial)	T_{STR}	-40 to + 85	℃
Relative Humidity (non-condensing)	H_{UM}	95 (maximum)	%

Table 5

***Comments**

Stress above those listed under " Absolute Maximum Ratings " may cause permanent damage to the products. These are stress rating only. Functional operation of these products at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Function Table

(Write is NOT protected)

Function	REG*	CE2*	CE1*	A0	OE*	WE*	WP	D15 - D8	D7 - D0
Read C/M (x8)	H	H	L	L	L	H	L	High - Z	Even Byte Data Out
Read C/M (x8)	H	H	L	H	L	H	L	High - Z	Odd Byte Data Out
Read C/M (x8)	H	L	H	X	L	H	L	Odd Byte Data Out	High - Z
Read C/M (x16)	H	L	L	X	L	H	L	Odd Byte Data Out	Even Byte Data Out
Write C/M (x8)	H	H	L	L	H	L	L	X	Even Byte Data In
Write C/M (x8)	H	H	L	H	H	L	L	X	Odd Byte Data In
Write C/M (x8)	H	L	H	X	H	L	L	Odd Byte Data In	X
Write C/M (x16)	H	L	L	X	H	L	L	Odd Byte Data In	Even Byte Data In
Standby	X	H	H	X	X	X	L	High - Z	High - Z
Output Disable	X	X	X	X	H	H	L	High - Z	High - Z
Read A/M (x8)	L	H	L	L	L	H	L	High - Z	Even Byte Data Out
Read A/M (x8)	L	H	L	H	L	H	L	High - Z	Data Out (invalid)
Read A/M (x8)	L	L	H	X	L	H	L	Data Out (invalid)	High - Z
Read A/M (x16)	L	L	L	X	L	H	L	Data Out (invalid)	Even Byte Data Out
Write A/M (x8)	L	H	L	L	H	L	L	X	Even Byte Data In
Write A/M (x8)	L	H	L	H	H	L	L	X	X
Write A/M (x8)	L	L	H	X	H	L	L	X	X
Write A/M (x16)	L	L	L	X	H	L	L	X	Even Byte Data In

Table 6

Function Table

(Write is protected)

Function	REG*	CE2*	CE1*	A0	OE*	WE*	WP	D15 - D8	D7 - D0
Read C/M (x8)	H	H	L	L	L	H	H	High - Z	Even Byte Data Out
Read C/M (x8)	H	H	L	H	L	H	H	High - Z	Odd Byte Data Out
Read C/M (x8)	H	L	H	X	L	H	H	Odd Byte Data Out	High - Z
Read C/M (x16)	H	L	L	X	L	H	H	Odd Byte Data Out	Even Byte Data Out
Write C/M (x8)	H	H	L	L	H	L	H	X	X
Write C/M (x8)	H	H	L	H	H	L	H	X	X
Write C/M (x8)	H	L	H	X	H	L	H	X	X
Write C/M (x16)	H	L	L	X	H	L	H	X	X
Standby	X	H	H	X	X	X	H	High - Z	High - Z
Output Disable	X	X	X	X	H	H	H	High - Z	High - Z
Read A/M (x8)	L	H	L	L	L	H	H	High - Z	Even Byte Data Out
Read A/M (x8)	L	H	L	H	L	H	H	High - Z	Data Out (invalid)
Read A/M (x8)	L	L	H	X	L	H	H	Data Out (invalid)	High - Z
Read A/M (x16)	L	L	L	X	L	H	H	Data Out (invalid)	Even Byte Data Out
Write A/M (x8)	L	H	L	L	H	L	H	X	X
Write A/M (x8)	L	H	L	H	H	L	H	X	X
Write A/M (x8)	L	L	H	X	H	L	H	X	X
Write A/M (x16)	L	L	L	X	H	L	H	X	X

Table 7

Definition : C/M = Common Memory, A/M = Attribute Memory

L = V_{IL}; H = V_{IH}; X = don't care can be either V_{IH} or V_{IL}

Common Memory Address Configuration Using 8-bit Data Bus (CE2*=VIH,CE1*=VIL)

A22 to A0	D15 -- D8	D7 -- D0
00 0000 0000 0000 0000 0000	High - Z	Address 0
00 0000 0000 0000 0000 0001	High - Z	Address 1
00 0000 0000 0000 0000 0010	High - Z	Address 2
↓	↓	↓
11 1111 1111 1111 1111 1101	High - Z	Address 8388605
11 1111 1111 1111 1111 1110	High - Z	Address 8388606
11 1111 1111 1111 1111 1111	High - Z	Address 8388607

Table 8

Common Memory Address Configuration Using 8-bit Data Bus (CE2*=VIL,CE1*=VIH)

A22 to A0	D15 -- D8	D7 -- D0
00 0000 0000 0000 0000 000X	Address 1	High - Z
00 0000 0000 0000 0000 001X	Address 3	High - Z
00 0000 0000 0000 0000 010X	Address 5	High - Z
↓	↓	↓
11 1111 1111 1111 1111 101X	Address 8388603	High - Z
11 1111 1111 1111 1111 110X	Address 8388605	High - Z
11 1111 1111 1111 1111 111X	Address 8388607	High - Z

Table 9

Common Memory Address Configuration Using 16-bit Data Bus (CE2*=VIL,CE1*=VIL)

A22 to A0	D15 -- D8	D7 -- D0
00 0000 0000 0000 0000 000X	Address 1	Address 0
00 0000 0000 0000 0000 001X	Address 3	Address 2
00 0000 0000 0000 0000 010X	Address 5	Address 4
↓	↓	↓
11 1111 1111 1111 1111 101X	Address 8388603	Address 8388602
11 1111 1111 1111 1111 110X	Address 8388605	Address 8388604
11 1111 1111 1111 1111 111X	Address 8388607	Address 8388606

Table 10

The above tables are examples for 8M bytes / 4M words SRAM cards.

Definition : L = VIL; H = VIH; X = don't care , can be either VIH or VIL.

DC Electrical Characteristics

(recommended operating conditions unless otherwise noted)

Symbol	Parameter		Min.	Max.	Unit	Test Conditions
I_{LI}	Input Leakage Current		-10	10	uA	V_{IN} = 0V to Vcc (Note 3)
			-70	10	uA	V_{IN} = 0V to Vcc (Note 4)
I_{LO}	Output Leakage Current		-10	10	uA	CE1* = CE2* = V_{IH} or OE* = V_{IH} , $V_{I/O}$ = 0V to V_{CC} (Note 1)
V_{OH}	Output High Voltage		3.8		V	I_{OH} = -2mA (Note 2)
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA (Note 2)
V_{IH}	Input High Voltage		0.7Vcc	Vcc+0.3	V	
V_{IL}	Input Low Voltage		-0.3	0.3Vcc	V	
I_{CC}	Vcc Operating Current			120	mA	Min. cycle , I_{Out} = 0mA
I_{SB}	Vcc Standby Current			0.1	mA	For page 3 & 4, item 9
	(CE1*= CE2*= V_{IH} or			0.2	mA	For page 3 & 4, item 10
	CE1*= CE2*≥VCC - 0.2V)			0.1	mA	For page 3 & 4, item 11
				0.2	mA	For page 3 & 4, item 12
				0.1	mA	For page 3 & 4, item 13
				0.2	mA	For page 3 & 4, item 14
				0.3	mA	For page 3 & 4, item 15
				0.3	mA	For page 3 & 4, item 16
				0.15	mA	For page 3 & 4, item 1
				0.25	mA	For page 3 & 4, item 2
				0.15	mA	For page 3 & 4, item 3
				0.25	mA	For page 3 & 4, item 4
				0.15	mA	For page 3 & 4, item 5
				0.25	mA	For page 3 & 4, item 6
				0.35	mA	For page 3 & 4, item 7
				0.35	mA	For page 3 & 4, item 8
I_{BU}	Battery Back-up Current	64KB		40	uA	1uA (Ta = 25℃)
	(All pins open , V_{BAT} = 3V	128KB		80	uA	2uA (Ta = 25℃)
	V_{CC} = 0V)	256KB		40	uA	1uA (Ta = 25℃)
		512KB		80	uA	2uA (Ta = 25℃)
		1MB		50	uA	1uA (Ta = 25℃)
		2MB		100	uA	2uA (Ta = 25℃)
		4MB		200	uA	4uA (Ta = 25℃)
		8MB		160	uA	4uA (Ta = 25℃)
V_{BDET1}	Battery Detect Reference Voltage 1		2.27	2.47	V	2.37V (Typ.) Vcc = 5V , Ta = 25℃
V_{BDET2}	Battery Detect Reference Voltage 2		2.55	2.75	V	2.65V (Typ.) Vcc = 5V , Ta = 25℃

Table 11

Note: 1.) Except BVD1*,BVD2*,CD1*,CD2* pins.
2.) Except CD1*,CD2* pins.
3.) Except CE1*,CE2*,WE*,REG* pins.
4.) For CE1*,CE2*,WE*,REG* pins.

AC Electrical Characteristics (Common Memory)

(recommended operating conditions unless otherwise noted)

Read Cycle (Common Memory)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{cr}	Read Cycle Time	150		ns	
$t_{a(A)}$	Address Access Time		150	ns	
$t_{a(CE)}$	Card Enable Access Time		150	ns	
$t_{a(OE)}$	Output Enable Access Time		75	ns	
$t_{dis(CE)}$	Output Disable Time (CE*)		75	ns	
$t_{dis(OE)}$	Output Disable Time (OE*)		75	ns	
$t_{en(CE)}$	Output Enable Time (CE*)	5		ns	
$t_{en(OE)}$	Output Enable Time (OE*)	5		ns	
$t_{v(A)}$	Data Hold Time (from address changed)	0		ns	

Table 12

Write Cycle (Common Memory)

Symbol	Parameter	Min.	Max	Unit	Test Condition
t_{cw}	Write Cycle Time	150		ns	
$t_{w(WE)}$	Write Pulse Width	80		ns	
tsu(A)	Address Setup Time	20		ns	
$t_{su(A-WEH)}$	Address Setup Time (WE*)	100		ns	
$t_{su(CE-WEH)}$	CE* Setup Time (WE*)	100		ns	
$t_{su(D-WEH)}$	Data Setup Time (WE*)	50		ns	
$t_{h(D)}$	Data Hold Time	20		ns	
$t_{rec(WE)}$	Write Recovery Time	20		ns	
$t_{dis(WE)}$	Output Disable Time (WE*)		75	ns	
$t_{dis(OE)}$	Output Disable Time (OE*)		75	ns	
$t_{en(WE)}$	Output Enable Time (WE*)	5		ns	
$t_{en(OE)}$	Output Enable Time (OE*)	5		ns	
$t_{en(OE-WE)}$	Output Enable Setup Time (WE*)	10		ns	
$t_{h(OE-WE)}$	Output Enable Hold Time (WE*)	10		ns	

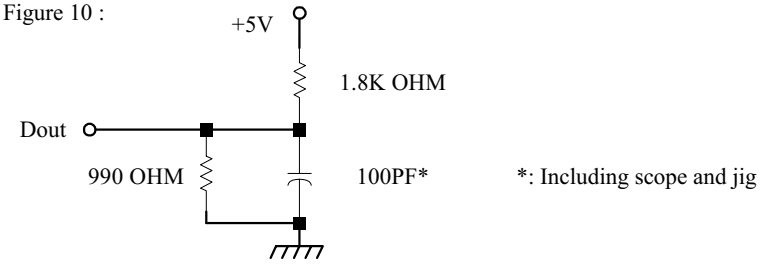
Table 13

AC Characteristics Test Conditions

Input Pulse Level	V_{OH} = 0.7Vcc , V_{IL}= 0.8V
Input Rise and Fall Time	5ns (max)
Timing Measurement Reference Level	V_{IH} / V_{IL} = 2.4V / 0.6V , V_{OH} / V_{OL} = 2V / 0.8V
Output Load	1TTL Gate + 100PF (Figure 9)

Table 14

Figure 10 :



Input / Output Capacitance

(Ta = 25蚓, f = 1MHZ,Vin/Vout = 0V) , these parameters are sampled not 100% tested.

Symbol	Parameter	Min.	Max.	Unit
Cin	Input Capacitance		110	PF
Ci/o	I/O Capacitance		35	PF

Table 15

Timing Diagram (Common Memory)

Read Cycle Timing Diagram (Common Memory) (WE*=REG*=V_{IH})

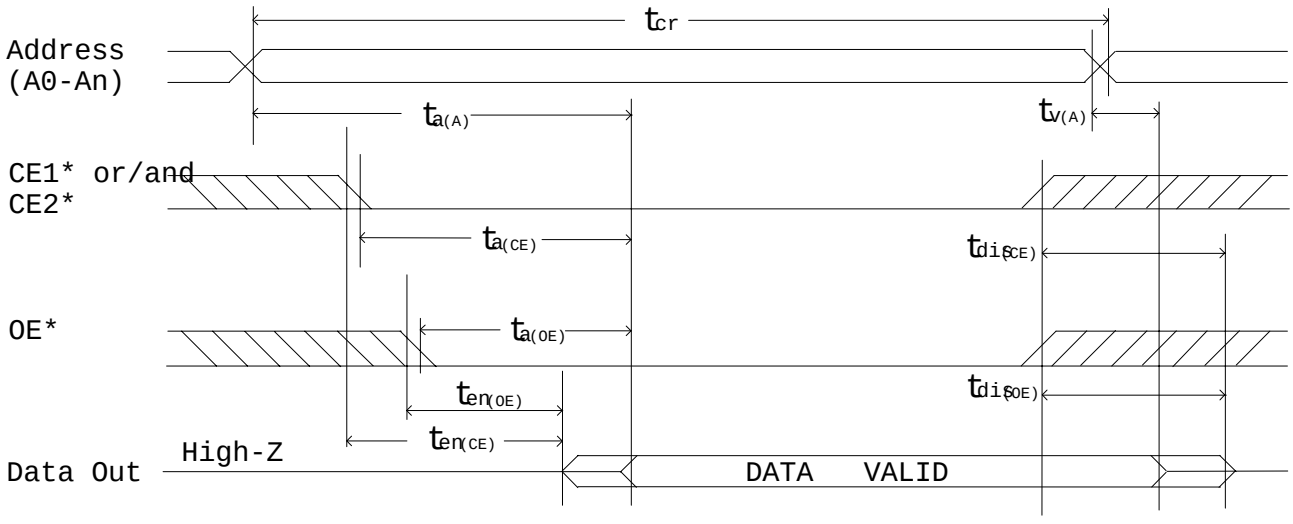


Figure 11

Note : 1) For 64KB , An = A15. 128KB , An = A16. 256KB , An = A17. 512KB , An = A18.
1MB , An = A19. 2MB , An = A20. 4MB , An = A21 8MB , An = A22.

2) The shaded area may be either high or low.

Write Cycle Timing Diagram (Common Memory) (REG*=V_{IH} , WE* controlled)

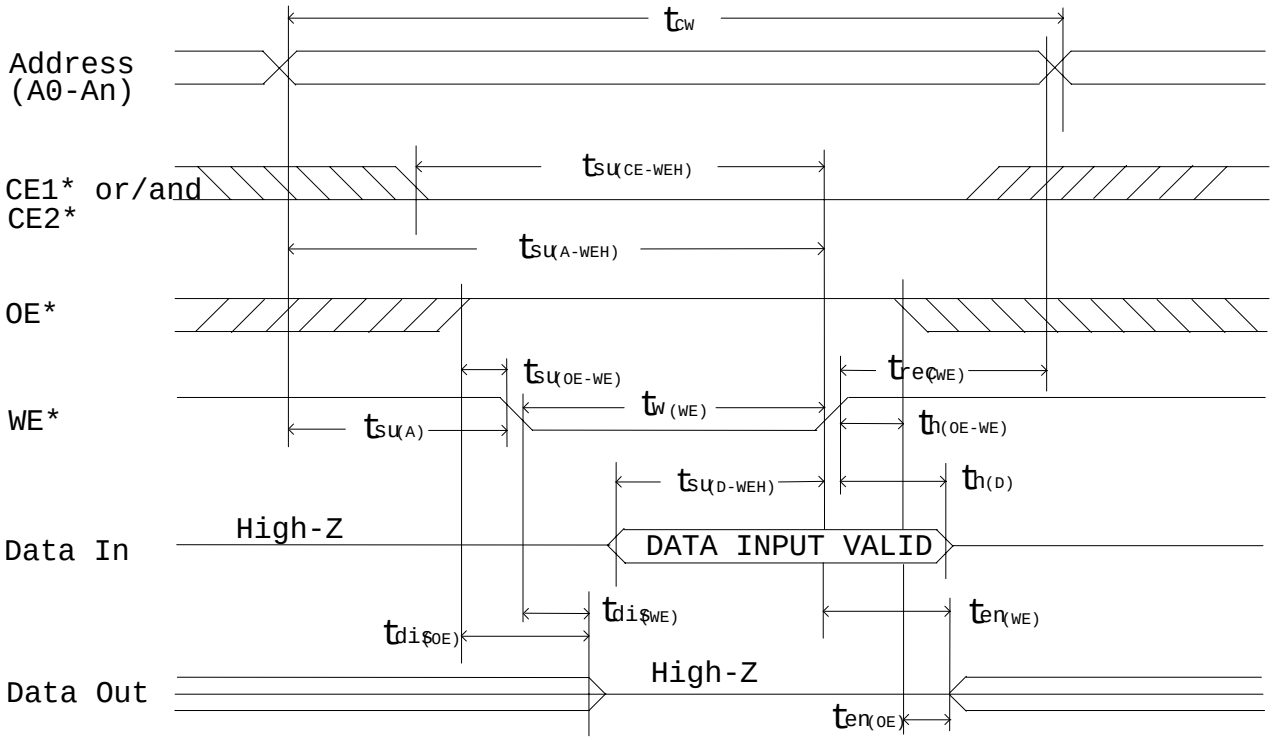


Figure 12

Write Cycle Timing Diagram (Common Memory) (CE* controlled , OE*=REG*=Vih)

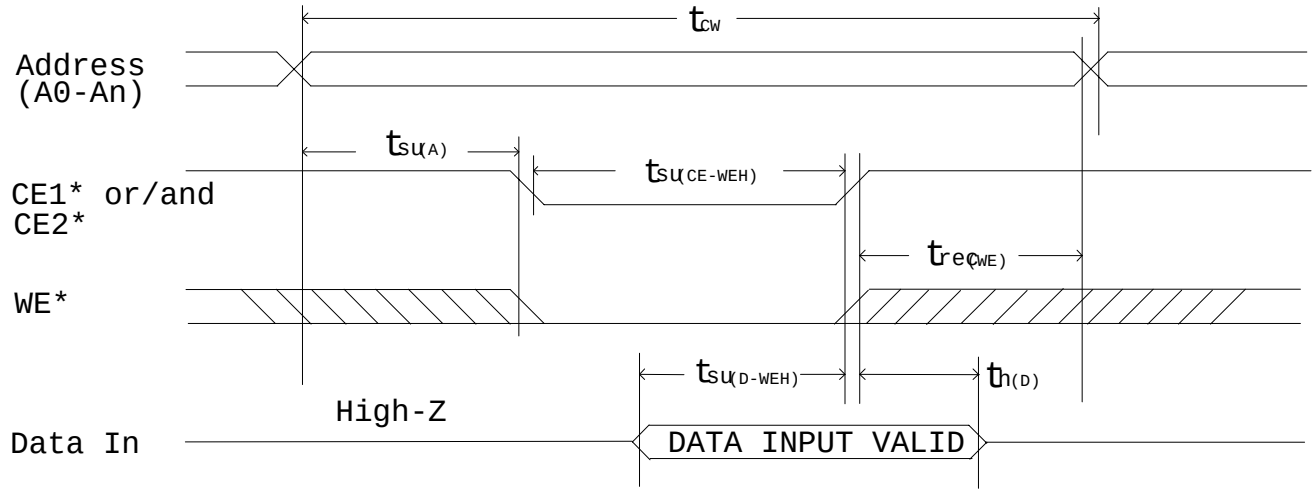


Figure 13

Note : 1) For 64KB , An = A15. 128KB , An = A16. 256KB , An = A17. 512KB , An = A18.
1MB , An = A19. 2MB , An = A20. 4MB , An = A21 8MB , An = A22.

2) The shaded area may be either high or low.

AC Electrical Characteristics (Attribute Memory)

(recommended operating conditions unless otherwise noted)

Read Cycle (Attribute Memory)

Symbol	Parameter	Min.	Max	Unit	Test Condition
t_{cr}	Read Cycle Time	300		ns	
$t_{a(A)}$	Address Access Time		300	ns	
$t_{a(CE)}$	Card Select Access Time		300	ns	
$t_{a(OE)}$	Output Enable Access Time		150	ns	
$t_{dis(CE)}$	Output Disable Time (from CE*)		100	ns	
$t_{dis(OE)}$	Output Disable Time (from OE*)		100	ns	
$t_{en(CE)}$	Output Enable Time (from CE*)	5		ns	
$t_{en(OE)}$	Output Enable Time (from OE*)	5		ns	
$t_{v(A)}$	Data Hold Time (from address changed)	0		ns	

Table 16

Write Cycle (Attribute Memory)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CW}	Write Cycle Time		1	ms	
t_{AS}	Address Setup Time	30		ns	
t_{AH}	Address Hold Time	50		ns	
t_{WP}	Write Pulse Width	120		ns	
t_{CS}	Card Enable Time to WE*	15		ns	
t_{CH}	Card Enable Hold Time from WE* High	0		ns	
t_{DS}	Data Setup Time	70		ns	
t_{DH}	Data Hold Time	30		ns	
t_{OES}	OE* Setup Time	30		ns	
t_{OEH}	OE* Hold Time	30		ns	
t_{DB}	Delay from WE* high to BUSY* Asserted		50	ns	

Table 17

Timing Diagram (Attribute Memory)

Read Cycle Timing Diagram (Attribute Memory) (REG*=VIL , WE*=VIH)

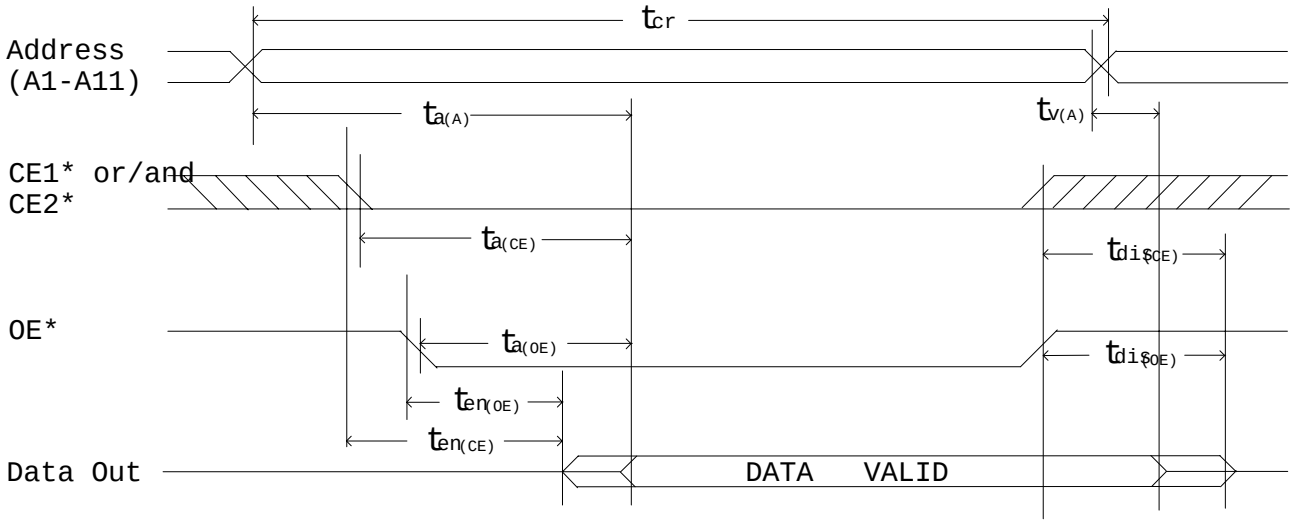


Figure 14

Write Cycle Timing Diagram (Attribute Memory) (REG*=VIL)

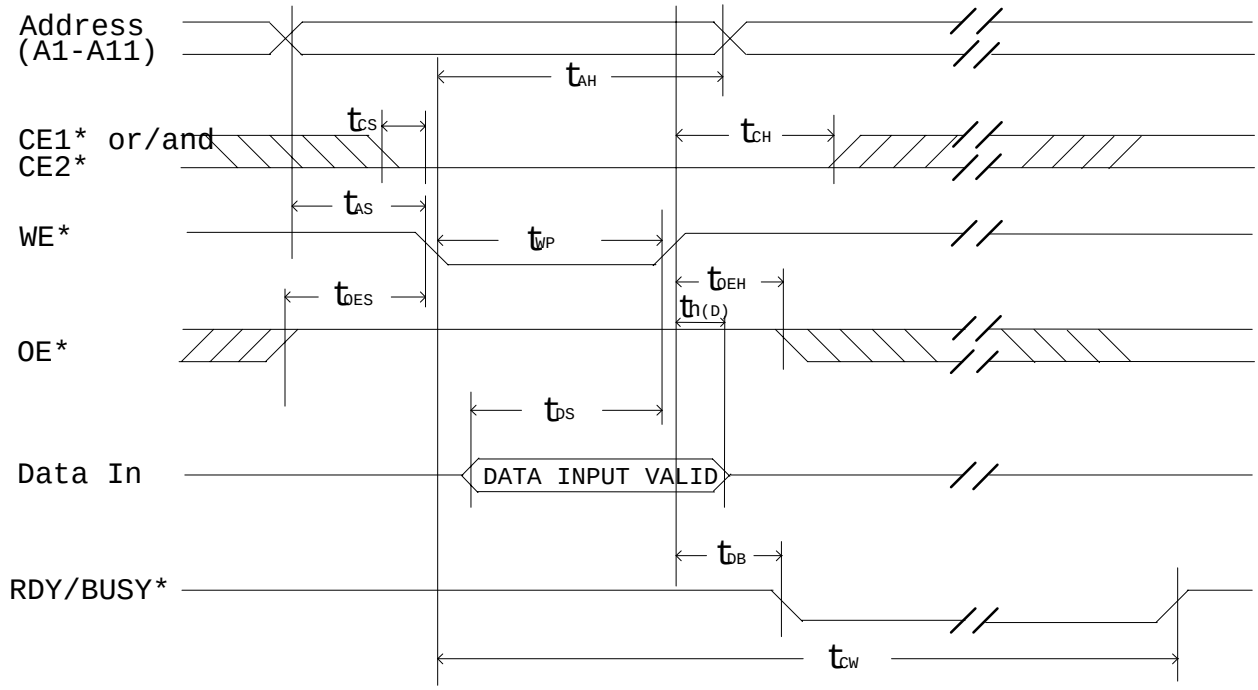


Figure 15

Battery Voltage Detection

BVD1*/BVD2* pins are used to monitor the voltage of the main battery which should be maintained at 2.65V or greater for data retention. The following table described the main battery status by reading the signals on BVD1*/BVD2* pins.

BVD1*	BVD2*	Main Battery	Comments
H	H	$V_{BAT} \geq 2.65V$	Data retention is OK. Battery is operational
H	L	$2.37V < V_{BAT} < 2.65V$	Data retention is OK. But battery should be replaced.
L	L	$V_{BAT} < 2.37V$	Data integrity is not guaranteed. Battery must be replaced.

Table 18

Note : if the main battery is removed , BVD1* and BVD2* pins will not function

Main Battery Specifications

■ 3V Lithium battery

Diameter	Thickness	Brand	Model No.
23.0mm	2.5mm	RAYOVAC	BR2325
		FDK	CR2325
		PANASONIC	BR2325

■ Recommended parts (Please refer to the table below)

Diameter	Thickness	Brand	Model No.
20.0mm	2.5mm	TOSHIBA	CR2025
		FDK	CR2025
		PANASONIC	CR2025

Approximate Battery Life Time Under Battery Back-up Only

(Ta=25°C, Humidity=60% R.H.) ∗battery life unit : year

Product Part No.	Battery Life	Product Part No.	Battery Life
SA5064C, SA5064I	6 / 4.5	SN5064C, SN5064I	6 / 4.5
SA5128C, SA5128I	4 / 3	SN5128C, SN5128I	4 / 3
SA5256C, SA5256I	6 / 4.5	SN5256C, SN5256I	6 / 4.5
SA5512C, SA5512I	4 / 3	SN5512C, SN5512I	4 / 3
SA501MC,SA501MI	6 / 4.5	SN501MC,SN501MI	6 / 4.5
SA502MC,SA502MI	4 / 3	SN502MC,SN502MI	4 / 3
SA504MC,SA504MI	2.5 / 2	SN504MC,SN504MI	2.5 / 2
SA508MC,SA508MI	2.5 / 2	SN508MC,SN508MI	2.5 / 2

Table 19

*For battery life , the numbers on the left-hand side of slash denote using 2325 series batteries. The numbers on the right-hand side of slash denote using 2025 series batteries.

Card Detection

CD1* , CD2* pins are used to detect the insertion of the card into the system. When the memory card has been correctly inserted , CD1* and CD2* are detected by the system . The recommended circuit in the system side is shown in figure below.

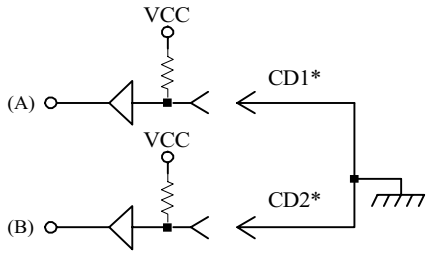


Figure 16

Power-up / Power-down Characteristics

Symbol	Parameter	Min.	Max.	Unit	Condition	Note
Vi(CE)	CE* Signal Level	0	ViMAX	V	0V ≤ VCC < 2.0	1
		VCC-0.1	ViMAX	V	2.0 ≤ VCC < V_{IH}	
		V_{IH}	ViMAX	V	V_{IH} ≤ VCC	
$t_{su(VCC)}$	CE* Setup Time	20		ms	10ms (Typ.)	
$t_{rec(VCC)}$	CE* Recovery Time	1		us		
t_{pr}	VCC Rising Time	0.1	300	ms	10% → 90% (VCC+5%)	1
t_{pf}	VCC Falling Time	3.0	300	ms	90% (VCC-5%) → 10%	1

Table20

Note:

1.) ViMAX means absolute maximum voltage for input.

2.) For the period 0V ≤ VCC< 2.0V , power supply voltage is low , so 0V~ ViMAX is permitted , because the logic for the system interface IC may not be determined.

3.) The Tpr and Tpfare defined as " linear waveform " in the period of 10% to 90%. Even if the waveform is not " linear waveform " , its rising and falling time must meet this specification.

Power-up Timing Diagram

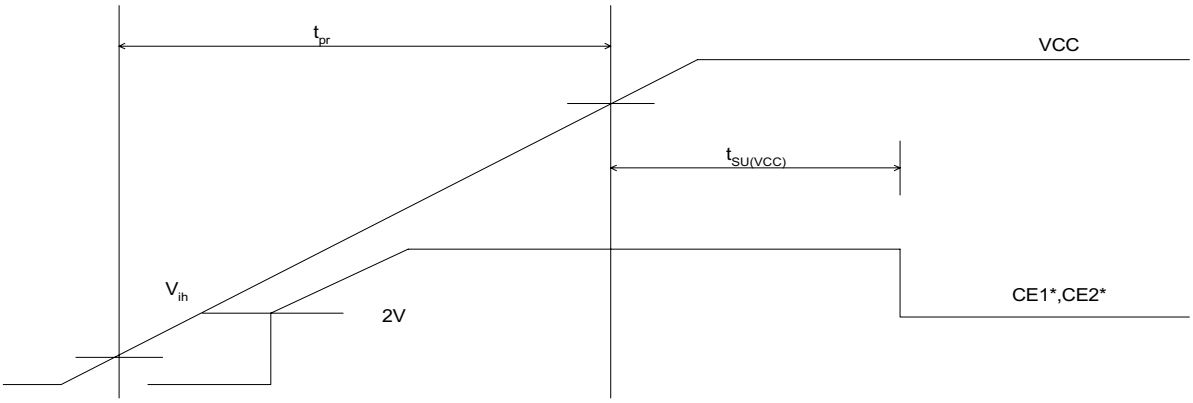


Figure 17

Power-down Timing Diagram

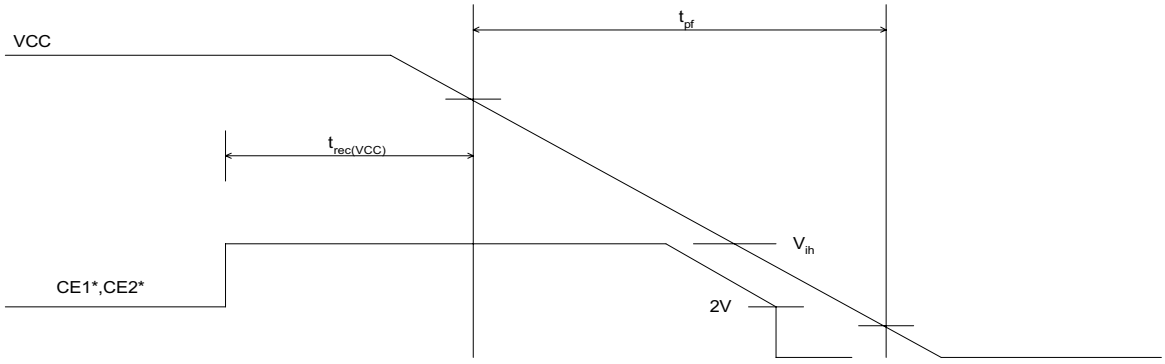


Figure 18

Outline Dimensions (Unit: mm)