OPERATOR'S MANUAL

# CM52
# Remote I/O
# Interface Module

Manual Revision 2, 8-98
Publication #17-1262

## Escort Memory Systems Warranty

Escort Memory Systems warrants that all products of its own manufacture conform to Escort Memory Systems specifications and are free from defects in material and workmanship when used under normal operating conditions and within the service conditions for which they were furnished. The obligation of Escort Memory Systems hereunder shall expire one (1) year after delivery, unless otherwise specified, and is limited to repairing, or at its option, replacing without charge, any such product which in Escort Memory Systems' sole opinion proves to be defective within the scope of this Warranty. In the event Escort Memory Systems is not able to repair or replace defective products or components within a reasonable time after receipt thereof, Buyers shall be credited for their value at the original purchase price. Escort Memory Systems must be notified in writing of the defect or nonconformity within the warranty period and the affected product returned to Escort Memory Systems factory or to an authorized service center within thirty (30) days after discovery of such defect or nonconformity. Shipment shall not be made without prior authorization by Escort Memory Systems.

This is Escort Memory Systems' sole warranty with respect to the products delivered hereunder. No statement, representation, agreement or understanding oral or written, made by an agent, distributor, representative, or employee of Escort Memory Systems which is not contained in this warranty, will be binding upon Escort Memory Systems, unless made in writing and executed by an authorized Escort Memory Systems employee. Escort Memory Systems makes no other warranty of any kind whatsoever, expressed or implied, and all implied warranties of merchantability and fitness for a particular use which exceed the aforestated obligation are hereby disclaimed by Escort Memory Systems and excluded from this agreement. Under no circumstances shall Escort Memory Systems be liable to Buyer, in contract or in tort, for any special, indirect, incidental, or consequential damages, expenses, losses or delay however caused.

Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Escort Memory Systems shall make the final determination as to the existence and cause of any alleged defect. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Escort Memory Systems in the contract for such custom equipment.

This warranty is the only warranty made by Escort Memory Systems with respect to the goods delivered hereunder, and may be modified or amended only by a written instrument signed by a duly authorized officer of Escort Memory Systems and accepted by the Buyer.



**Escort Memory Systems, Inc.**
**A Datalogic Group Company**
3 Victor Square
Scotts Valley, CA 95066
Telephone (831) 438-7000
FAX (831) 438-5768
www.ems-rfid.com

# TABLE OF CONTENTS

# 1 INTRODUCTION

## 1.1 CM52 Description

The CM52 Remote I/O (RIO) module is a general purpose programmable interface between the Allen-Bradley (A-B) Remote I/O network and Escort Memory Systems' RFID (Radio Frequency Identification) equipment, or third party products. The CM52 interfaces to a variety of devices: two EMS HS/HL500-Series antennas; two HMS8xx series antennas; two serial ports; and as many as 32 HMS-Series Reader/Writers, RS-Series Read Only antennas, or bar code scanners (or combinations) on an RS485 MUX32 line.

The CM52 is housed in a NEMA 2 enclosure suitable for light-industrial and commercial applications, and is DIN rail mountable with optional clips (00-1096).

The CM52 is a slave device that supports RIO protocol at communication speeds of 57.6K, 115.2K or 230.4K bits-per-second and is therefore compatible with all RIO scanners.

This programmable interface is provided with a standard program that allows RIO commands to control the reading and writing of a block (or non-contiguous blocks) of data, MUX32 connection status, serial inputs and outputs, and fill functions. Custom application programs can be written and downloaded to the CM52. Please contact your Escort Memory Systems (EMS) representative for assistance if modification to the Standard Program is needed.

Power for the CM52 is supplied by an external power supply. All device I/O is electrically isolated from the Remote I/O bus.

The CM52 is equipped with three microprocessors:

- The node adapter chip processor, to interface with the Remote I/O bus
- An RF coprocessor, to read and write tags.
- A powerful 386EX main processor to manage serial I/O and the RF commands

To facilitate control, the main processor utilizes a real-time operating system. Using this approach, up to four tasks may execute concurrently. With a real-time operating system and separate coprocessors, it is possible to simultaneously write data on a serial port, read a tag, and handle bus traffic.

Special commands have been implemented to improve throughput when reading large tags. The data on the tag is first read into a buffer on the CM52. Subsequent commands transfer the data in the buffer, across the bus, to the host. A 16K buffer is available to hold the data for each task.

The CM52 has several possible RFID configurations. It may be connected to two HS-Series Antennas through its antenna ports or to HMS-Series Passive Reader/Writers or RS Series Read Only devices via the serial ports. The CM52 can transfer 3000 bytes per second to or from HS-Series tags. Using the long range tags HS tags, the distance from the antenna to the tag can be 20 inches.

# 2 INSTALLATION

## 2.1 Mechanical Dimensions

Below are the mechanical dimensions of the CM52 and the optional DIN rail clips.

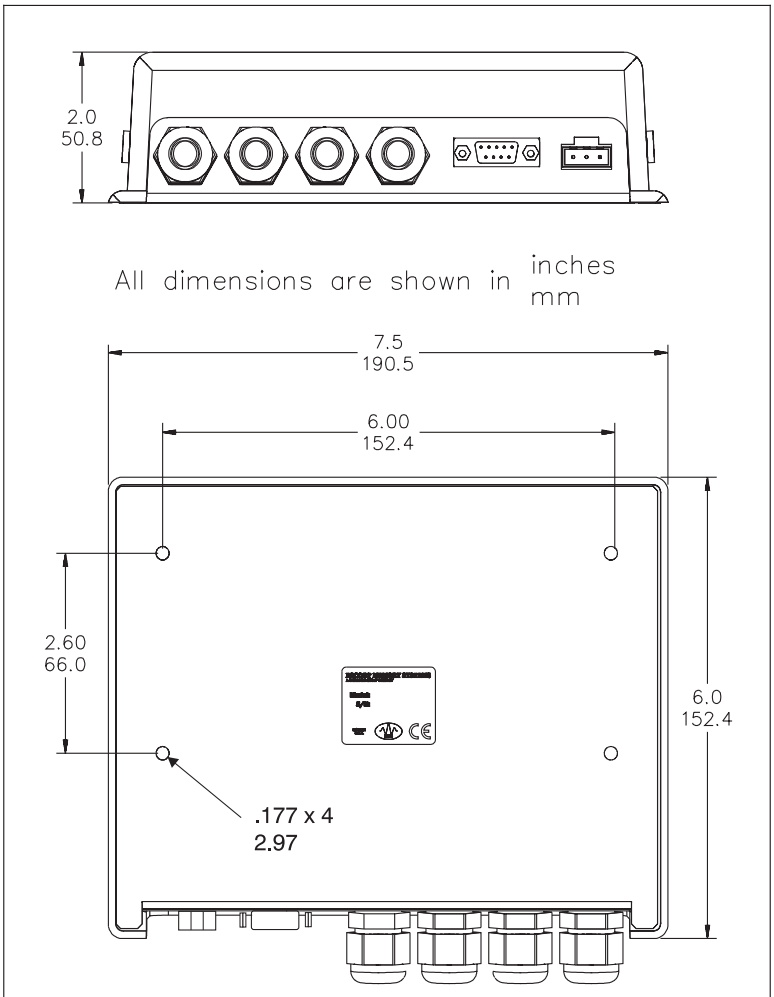


**Figure 1 — CM52 Dimensions**

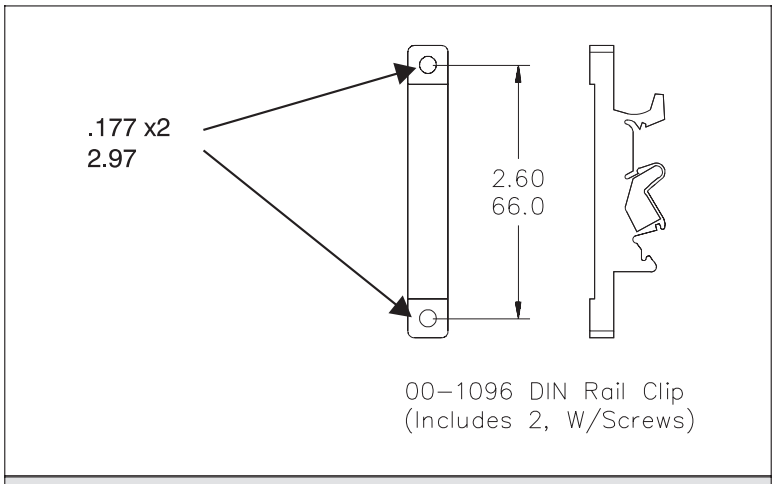


**Figure 2 — CM52 DIN Rail Clip**

## 2.2 Connectors

### Connector Panel

Only the Remote I/O connector and a standard DB9 connector for COM1 are mounted externally. All other connections are made on the terminal strip connector inside the CM52 and accessed through the cable grips.

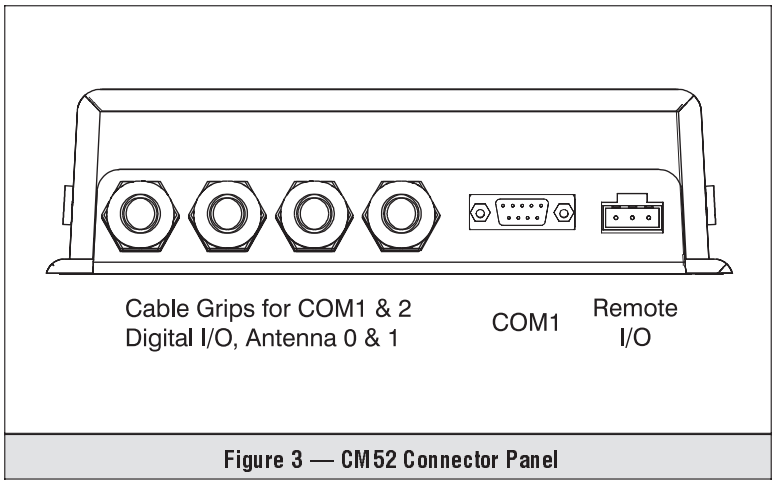


**Figure 3 — CM52 Connector Panel**

### Remote I/O Connector

The CM52 RIO connector is a female three-pin screw-terminal connector that is the standard Remote I/O connector. Nodes are linked by daisy-chaining two signal wires and a shield conductor from these connectors. Typically the blue wire is Pin 1 and the clear wire is Pin 3 with the shield in the center on Pin 2. On the CM52, this connector is externally accessible.

**Table 1 — Remote I/O Pinouts**

| Terminal | Description |
|---|---|
| 1 | Line 1 - Blue wire (+) |
| 2 | Shield |
| 3 | Line 2 - Clear wire (-) |

### COM1 Connector

The DB9 connector simplifies the connection of a host to the COM1 serial interface. The pinouts are standard and provided in Table 2 for your convenience. Signal names are relative to the CM52.

**Table 2 — COM1 Pinouts**

| Pin | Description |
|---|---|
| 2 | RS232 TX |
| 3 | RS232 RX |
| 5 | Signal Ground |

All other pins are no connects.

### Internal Connections

To access the internal connectors, switches, and jumpers, first turn off power to the module. Next, loosen the two thumbscrews which hold the cover tot he base plate, Then remove the cover. Observe standard ESD procedures to protect circuits from damage.

All connections are made to screw-type terminal blocks with cable clamps provided to physically retain the cabling. Figure 4 shows terminal block and the signal designations.

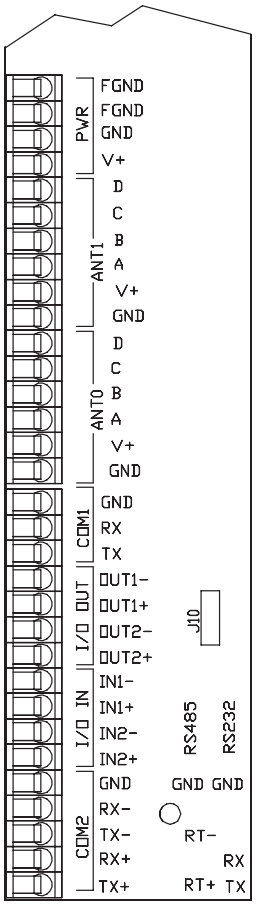


**Figure 4 — CM52 Internal Connector**

## 2.3 Cables

Use 1770-CD (Belden 9463) cable and connect a Remote I/O network using a daisy chain or trunk line/drop line configuration.

For daisy chain configurations, use the following table to determine the total cable length you can use.

**Table 3 — Cable Lengths**

| Communication Rate | Length |
|---|---|
| 57.6 kbps | 3,048 m (10,000 ft) |
| 115.2 kbps | 1,524 m (5,000 ft) |
| 230.4 kbps | 762 m (2,500 ft) |

## 2.4 Bus Termination

For proper operation terminate both ends of the Remote I/O link by placing an external resistor across the two signal wires at the three-pin connectors. Table 4 shows the proper resistor value that should be used for a particular RIO link configuration.

**Table 4 — Remote I/O Pinouts**

| Remote I/O Link Configuration | Resistor Rating | Maximum Number of Devices on the Link |
|---|---|---|
| Operating at 230.4 kbps | 82 ohms | 32 |
| Operating at 57.6 kbps or 115.2 kbps and no devices requiring 150 ohm resistors are on the link | 82 ohms | 32 |
| Devices requiring 150 ohm resistors are on the link | 150 ohms | 16 |
| Operating at 57.6 kbps or 115.2 kbps and link does not need to support more than 16 devices | 150 ohms | 16 |

## 2.5 Internal Switches and Jumpers

To access the internal switches and jumpers remove power from the module. Next, loosen the screws that hold the cover to the body, then remove the cover. Observe standard ESD procedures to protect circuits from damage.

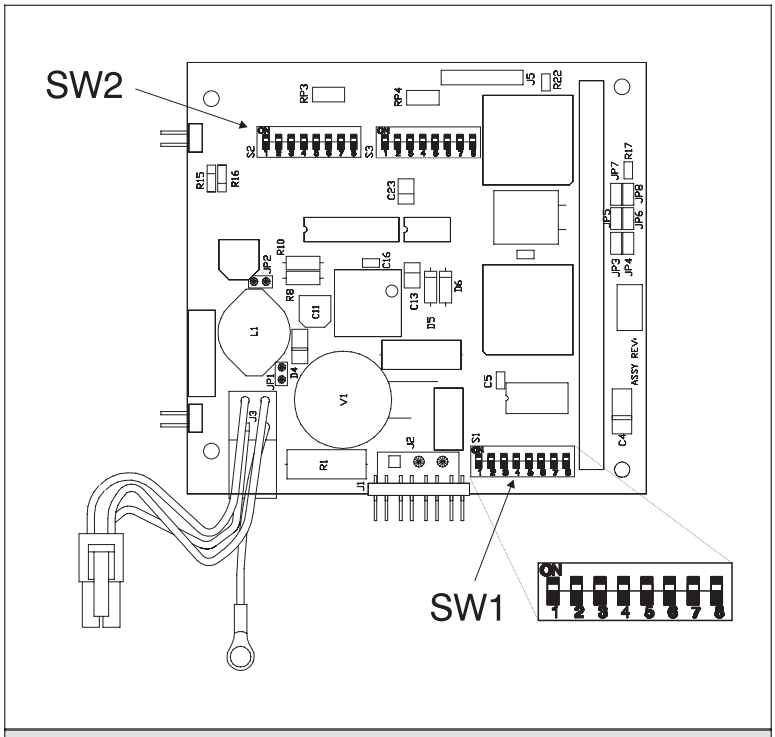


**Figure 5 — CM52 DIP Switches**

User-configurable RIO bus parameters are set with bit switches on the RIO interface board (the top board of the two-board CM52 stack). There are three banks of bit switches with definitions as follows:

| Switch Bank | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|
| SW1 | Rack Address | | | | | | Starting Quarter | |
| SW2 | Display Banner | reserved | reserved | Rack Size | reserved | Last Rack | Baud Rate | |
| SW3 | reserved | | | | | | | |

Details of each field setting are given in the sections below. Switch numbers and the meaning of each possible combination are shown. Note that ON and Off correspond to the labeled ON and OFF position on the switches themselves.

### Rack Address Switch Settings

Table 5 shows the switch configuration for all possible Rack Addresses from 0 to 59. Shaded areas indicate switches in the OFF position.

**Table 5 — Switch Settings for RIO Address**

| Rack Address | | SW1 DIP Switches | | | | | | Rack Address | | SW1 DIP Switches | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dec | HEX | 8 | 7 | 6 | 5 | 4 | 3 | Dec | HEX | 8 | 7 | 6 | 5 | 4 | 3 |
| 0 | 00 | | | | | | | 30 | 1E | | ON | ON | ON | ON | |
| 1 | 01 | | | | | | ON | 31 | 1F | | ON | ON | ON | ON | ON |
| 2 | 02 | | | | | ON | | 32 | 20 | ON | | | | | |
| 3 | 03 | | | | | ON | ON | 33 | 21 | ON | | | | | ON |
| 4 | 04 | | | | ON | | | 34 | 22 | ON | | | | ON | |
| 5 | 05 | | | | ON | | ON | 35 | 23 | ON | | | | ON | ON |
| 6 | 06 | | | | ON | ON | | 36 | 24 | ON | | | ON | | |
| 7 | 07 | | | | ON | ON | ON | 37 | 25 | ON | | | ON | | ON |
| 8 | 08 | | | ON | | | | 38 | 26 | ON | | | ON | ON | |
| 9 | 09 | | | ON | | | ON | 39 | 27 | ON | | | ON | ON | ON |
| 10 | 0A | | | ON | | ON | | 40 | 28 | ON | | ON | | | |
| 11 | 0B | | | ON | | ON | ON | 41 | 29 | ON | | ON | | | ON |
| 12 | 0C | | | ON | ON | | | 42 | 2A | ON | | ON | | ON | |
| 13 | 0D | | | ON | ON | | ON | 43 | 2B | ON | | ON | | ON | ON |
| 14 | 0E | | | ON | ON | ON | | 44 | 2C | ON | | ON | ON | | |
| 15 | 0F | | | ON | ON | ON | ON | 45 | 2D | ON | | ON | ON | | ON |
| 16 | 10 | | ON | | | | | 46 | 2E | ON | | ON | ON | ON | |
| 17 | 11 | | ON | | | | ON | 47 | 2F | ON | | ON | ON | ON | ON |
| 18 | 12 | | ON | | | ON | | 48 | 30 | ON | ON | | | | |
| 19 | 13 | | ON | | | ON | ON | 49 | 31 | ON | ON | | | | ON |
| 20 | 14 | | ON | | ON | | | 50 | 32 | ON | ON | | | ON | |
| 21 | 15 | | ON | | ON | | ON | 51 | 33 | ON | ON | | | ON | ON |
| 22 | 16 | | ON | | ON | ON | | 52 | 34 | ON | ON | | ON | | |
| 23 | 17 | | ON | | ON | ON | ON | 53 | 35 | ON | ON | | ON | | ON |
| 24 | 18 | | ON | ON | | | | 54 | 36 | ON | ON | | ON | ON | |
| 25 | 19 | | ON | ON | | | ON | 55 | 37 | ON | ON | | ON | ON | ON |
| 26 | 1A | | ON | ON | | ON | | 56 | 38 | ON | ON | ON | | | |
| 27 | 1B | | ON | ON | | ON | ON | 57 | 39 | ON | ON | ON | | | ON |
| 28 | 1C | | ON | ON | ON | | | 58 | 3A | ON | ON | ON | | ON | |
| 29 | 1D | | ON | ON | ON | | ON | 59 | 3B | ON | ON | ON | | ON | ON |

### Starting Quarter Switch Settings

The group address is determined by selecting a starting rack quarter for the CM52. Note that if the CM52 is configured as a half-rack device it cannot start at the fourth quarter. In such a case, if the fourth quarter is selected, the CM52 will change the starting quarter internally to the third quarter and print an error message to COM1 at startup (if the Display Banner bit switch is ON).

**Table 6 — Starting Quarter Switch Settings**

| Starting Quarter | Group Number | SW1 DIP Switch Settings | |
|---|---|---|---|
| | | 2 | 1 |
| First Quarter | Group 0 | OFF | OFF |
| Second Quarter | Group 2 | OFF | ON |
| Third Quarter | Group 4 | ON | OFF |
| Fourth Quarter | Group 6 | ON | ON |

### Baud Rate Switch Settings

One of three baud rates is selectable. Note that if switch 2 is ON, switch 1 is ignored.

**Table 7 — Baud Rate Switch Settings**

| Baud Rate | SW2 DIP Switch Settings | |
|---|---|---|
| | 2 | 1 |
| 57.6 Kbits/sec | OFF | OFF |
| 115.2 Kbits/sec | OFF | ON |
| 230.4 Kbits/sec | ON | OFF |

### Last Rack Switch Settings

In a PLC-2 system, this switch should be ON if the CM52 is the highest group in its rack address.

**Table 8 — Last Rack DIP Switch**

| Last Rack (SW2) | DIP Switch 3 |
|---|---|
| CM52 is not the highest group in this rack address | OFF |
| CM52 is the highest group in this rack address | ON |

### Rack Size Switch Settings

The Rack Size switch configures the CM52 as a 1/4 rack or 1/2 rack device.

**Table 9 — Rack Size DIP Switch**

| Rack Size (SW2) | DIP Switch 5 |
|---|---|
| Quarter Rack | OFF |
| Half Rack | ON |

### Display Banner Switch Setting

The Display Banner switch enables or disables transmission of the startup banner when the CM52 is powered-up or reset. If the switch is OFF nothing is printed on COM1. If the switch is ON various CM52 configuration information is printed including the version number for internal software modules, the RIO baud rate and address settings and any configuration errors or warnings that occur at startup.

**Table 10 — Display Banner DIP Switch**

| Display Banner (SW2) | DIP Switch 8 |
|---|---|
| No Banner Display | OFF |
| Banner Display | ON |

**Default Settings**

The CM52 is shipped with all switches in the off position with the resulting configuration:

| | |
|---|---|
| Rack Address | 0 |
| Group Address | 0 |
| Baud Rate | 57.6 Kbps |
| Last Rack | NO |
| Rack Size | Quarter Rack |
| Banner Display | None |

## 2.6 Jumpers

There are two selectable jumpers (J7 and J12) located on the CM52 Controller Board as illustrated below in Figure 6.

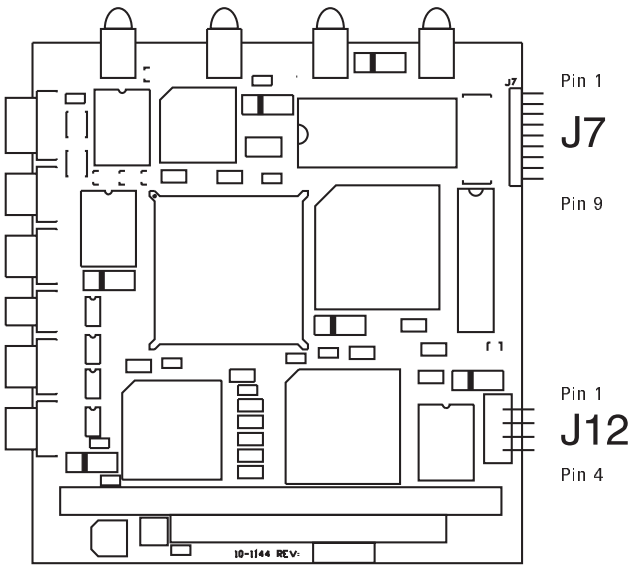


**Figure 6 — CM52 Controller Board Jumpers**

### J7 — COM2 RS232/RS485/RS422 Selection

Jumper J7 on the Controller board selects the serial communication protocol. The default setting configures the CM52 for communication with devices supporting RS232 protocol. For RS485/MUX 32 or RS422 protocol configure J7 as shown below in Figure 7.

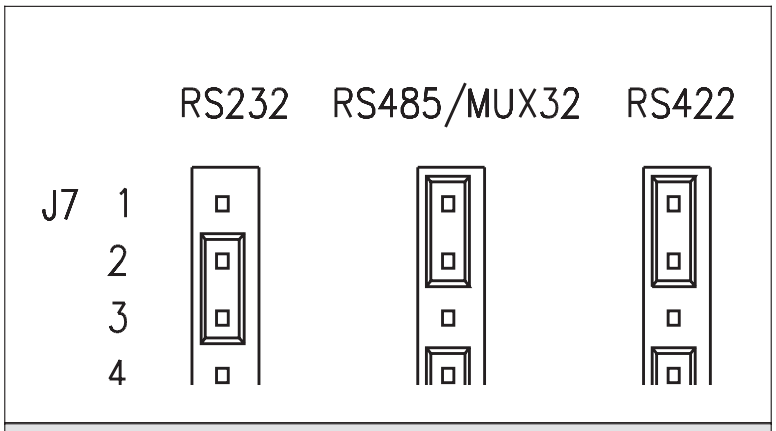


Figure 7 — Jumper Settings

**NOTE:**
For proper serial port communications, all of the following items must be properly configured:

- Jumpers
- Serial Parameters
- Output pin or terminal connections

### J12 — Run/Re-program Reset

This jumper is used to re-program and test the CM52. You will not need to change the settings of this jumper if you are using the Standard Program. If you wish to modify the Standard Program, contact your Escort Memory Systems representative for assistance.

## 2.7 LED Indicators

The CM52 has six LED indicators on the front panel as shown in Figure 8.

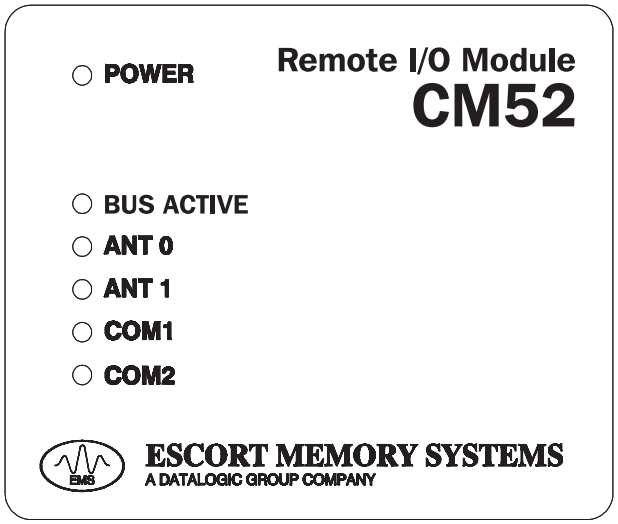


Figure 8 — CM52 LED Indicators

The LEDs colors and meanings are explained in Table 11 below.

Table 11 — CM52 LED Indicators

| LED | Color | Indicates |
|---|---|---|
| Power | Green | The CM52 has power |
| Bus Active | Green | There is activity in the bus. See below for explanation. |
| ANT 0 | Red | Antenna port 0 is active |
| ANT 1 | Red | Antenna port 1 is active |
| COM1 | Green | Serial communications port 1 is active |
| COM2 | Green | Serial communications port 2 is active |

### Bus Active LED

The green Bus Active LED provides status information and will always be in one of three states. Table 12 below explains what each LED state indicates.

**Table 12 — Bus Active LED**

| LED State | Indication |
|---|---|
| Off | CM52 bus processor has reset and is not initialized.<br>CM52 is not receiving valid frames from the scanner.<br>A communications timeout occurred, communications have not resumed. |
| Blinking | PLC is in program mode.<br>Communications have been established.<br>A communications timout, communications have resumed, bus processor has not been reinitialized. |
| On | Normal I/O commands are being received. |

### Possible Causes of LED Remaining OFF

- Reversed Remote I/O Line 1 and Line 2 connections.
- Incorrect data rate.
- Incorrect link address.

### Possible Causes of Frequent Bus Retries

- Absence or inappropriate placement of terminating resistors
- Incorrect terminator values (particularly important above 57.6 Kbps)

# 3 REMOTE I/O INTERFACE

## 3.1 Overview

The CM52 connects over the Remote I/O network to Allen-Bradley PLCs and Remote I/O scanner modules. The link supports remote, time-critical, I/O and control communications.

Remote I/O (RIO) is a proprietary network used to communicate between Allen-Bradley (A-B) PLCs and remote I/O racks and other devices. The RIO link is a time-division multiplexed, bit-synchronous, byte-oriented serial communication protocol based on SDLC packet formats. RIO is typically used to transfer I/O bit images between a processor and its remote, discrete I/O interface cards, or to transfer blocks of data between a processor and intelligent I/O cards.

RIO is a master-slave network, meaning the PLC scanner acts as the master initiating messages while slaves reply. Only one master is allowed on the network. Slave devices can be physical racks with remote I/O adapters, block I/O modules, operator interfaces, flex I/O, PLCs in adapter mode, and devices using the A-B node adapter chipset (CM52).

PC-based RIO cards are available complete with substantial driver support.

The node adapter chip set is designed to connect a host processor as an adapter-mode device to the RIO master PLC. In such a case, the node adapter appears as a rack of I/O.

The link operates at one of three data rates: 57.6K, 115.2K or 230.4K bits per second.

RIO supports 16 nodes at 57.6Kbps at 10,000 feet, or 16 nodes at 115.2Kbps at 5,000 feet, or 32 nodes at 230.4Kbps at 2,500 feet.

### 3.1.1 Device Addressing

Remote I/O devices are addressed by logical rack and logical group. A node adapter device like the CM52, uses two-slot addressing in which two slots are addressed as one logical group.

A ***rack***, as defined by the CM52 node adapter, consists of 16 slots with one byte of discrete input and output data associated with each slot. The rack address can range from 0 to 59 (00 to 3B hex)

A ***group*** consists of two slots and has one word (16 bits) of I/O associated with it. There are eight possible groups per rack. A quarter-rack device occupies two groups. The first quarter-rack begins at group 0, the second quarter at group 2, the third quarter at group 4 and the final quarter at group 6.

A device on the RIO link may be configured as a quarter, half, three quarter, or full-rack with the corresponding amount of discrete data associated with it. Furthermore, each partial rack device may be configured to "start" at a particular group address. The starting group address may be limited due to the rack size.

During each RIO scan, the scanner updates the appropriate number of input and output words associated with each device on the RIO bus. These I/O words (data) are mapped into the PLC Input and Output files according to the rack and group number. For instance, a half-rack device at Rack 3: Group 2 would map its inputs and outputs to I:032 - I:035 and O:032 - O:035, respectively.

The chart below shows the input and output data buffers and how they relate to slots, groups and various rack sizes. In this example a rack address of 3 is assumed. The shaded areas under the various rack sizes indicate the number of I/O bytes allocated to a device of that size.

| 1/4 Rack | 1/2 Rack | 3/4 Rack | Full Rack | Group | Slot | Input Data (Bytes) | Output Data (Bytes) |
|---|---|---|---|---|---|---|---|
| | | | | 0 | 0 | I:030 LSB | O:030 LSB |
| | | | | | 1 | I:030 MSB | O:030 MSB |
| | | | | 1 | 2 | I:031 LSB | O:031 LSB |
| | | | | | 3 | I:031 MSB | O:031 MSB |
| | | | | 2 | 4 | I:032 LSB | O:032 LSB |
| | | | | | 5 | I:032 MSB | O:032 MSB |
| | | | | 3 | 6 | I:033 LSB | O:033 LSB |
| | | | | | 7 | I:033 MSB | O:033 MSB |
| | | | | 4 | 8 | I:034 LSB | O:034 LSB |
| | | | | | 9 | I:034 MSB | O:034 MSB |
| | | | | 5 | 10 | I:035 LSB | O:035 LSB |
| | | | | | 11 | I:035 MSB | O:035 MSB |
| | | | | 6 | 12 | I:036 LSB | O:036 LSB |
| | | | | | 13 | I:036 MSB | O:036 MSB |
| | | | | 7 | 14 | I:037 LSB | O:037 LSB |
| | | | | | 15 | I:037 MSB | O:037 MSB |

If the RIO device was configured as a full rack it would have 16 bytes of discrete input and output data and would have to start at the first quarter, group 0. With other size configurations, the starting location is selectable. For example, a half-rack device could be configured to start at Group 0, 2, or 4 but not 6.

Generally, A-B PLCs support auto-configuration in which the RIO scanner automatically detects the number and configuration of all nodes on the bus.

### *3.1.2 Data Transfer*

The scanner exchanges data with an RIO device by two methods: discrete commands and block transfer commands.

***Discrete Commands*** occur constantly as the scanner exchanges discrete I/O buffers with each slave once per RIO scan. The number of bytes swapped with each device depends on the rack size configuration of that device.

***Block Transfer Commands*** are not scanned repeatedly, but are under PLC program control and typically limited to one transfer per rack per RIO scan. They can transfer up to 64 words (128 bytes) of data. When executing Block Transfers, the scanner makes use of the first byte of the discrete data areas for handshaking and status. Therefore, since the CM52 makes use of Block Transfers this byte is not available for I/O data.

Block Transfers can only be performed on the first slot of the first module group of the logical rack address space occupied by the CM52.

## 3.2 Command and Response Structure

CM52 commands and their responses are transmitted using a combination of discrete and block transfer data. The ***Parameters*** and data associated with a command are downloaded using a Block Transfer Write (BTW) instruction. The ***Flags*** that initiate commands and provide command status are bit-mapped in discrete I/O memory. Any data returned by the CM52 is retrieved using a Block Transfer Read (BTR) instruction.

Once a set of command parameters is downloaded to the CM52 using a Block Transfer Write function, a handshake sequence is executed using various Flags to ensure proper execution of the command.

In general, write commands require only a status response from the CM52 while read commands require the return of both status flags and data. Status responses involve only flags in the discrete input data while a data response also requires a Block Transfer Read.

### 3.2.1 Command and Response Flags (Discrete Data)

The bits used for the Command and Response flags are the same for all CM52 commands. As part of the PLC discrete I/O data these bytes are constantly exchanged between the CM52 and the PLC by the RIO scanner. Thus, they may be read or written by the PLC without issuing any commands to the CM52.

The number of discrete I/O bytes exchanged with the CM52 will depend on whether the CM52 is configured as a 1/4 or 1/2 rack device. This makes no difference for the Command flags but does have an effect on the amount of status information returned in the response flags. For both Command and Response Flags the first byte is reserved for scanner Block Transfer control and is unavailable to the CM52.

See the section titled "PLC Memory Mapping" for examples of how the Command and Response Flags map to specific PLC I/O registers.

**Command Flags (Discrete Data)**

The ***Command Flags*** include bits to set the state of the two digital outputs and the Initiate bit used to start a command execution in the CM52.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | |
| | MSB | Reserved by the CM52 | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

**Initiate Bit**

The Initiate bit is used to start the CM52 executing the last command received from the PLC via a Block Transfer Write command. The CM52 will begin execution and respond by setting the Acknowledge bit in the Response Flags.

**Digital Output Pins**
The two Digital Outputs Pin bits can be used to change the electrical state of the output points. Placing a "1" in these bits will complete an output circuit.

**Response Flags (Discrete Data)**

The ***Response Flags*** contain the Task Done bits, the command status bits, the digital input state bits and the MUX32 Data Ready bits. Unlike the Command Flags, the Response Flags are affected by the rack size of the CM52. The first four bytes are the same for either rack size, but if the CM52 is configured as a half-rack device, three additional bytes of status flags can be returned. These status bytes contain Data Ready flags for MUX32 device addresses 8 – 31.

Therefore, there is a trade-off between I/O space used by the CM52, and the number of MUX32 devices supported. If more than eight MUX32 devices are connected, the CM52 must be configured as a half-rack.

If eight or less MUX32 devices are needed, the CM52 can be configured as a 1/4 rack saving 16 bits of I/O with no loss of functionality.

In the table below, the last two words represents the additional bytes that would be defined if the CM52 were configured as a 1/2 rack. The eighth byte is not used. Bit numbers in the charts below use octal notation.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital Input 2 | Digital Input 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Data Ready | MUX32 Addr 06 Data Ready | MUX32 Addr 05 Data Ready | MUX32 Addr 04 Data Ready | MUX32 Addr 03 Data Ready | MUX32 Addr 02 Data Ready | MUX32 Addr 01 Data Ready | MUX32 Addr 00 Data Ready |
| If you have configured the CM52 as a 1/2 rack device, the following bytes will also be in the response. | | | | | | | | | |
| Word 2 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | MUX32 Addr 15 Data Ready | MUX32 Addr 14 Data Ready | MUX32 Addr 13 Data Ready | MUX32 Addr 12 Data Ready | MUX32 Addr 11 Data Ready | MUX32 Addr 10 Data Ready | MUX32 Addr 09 Data Ready | MUX32 Addr 08 Data Ready |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 23 Data Ready | MUX32 Addr 22 Data Ready | MUX32 Addr 21 Data Ready | MUX32 Addr 20 Data Ready | MUX32 Addr 19 Data Ready | MUX32 Addr 18 Data Ready | MUX32 Addr 17 Data Ready | MUX32 Addr 16 Data Ready |
| Word 3 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | MUX32 Addr 31 Data Ready | MUX32 Addr 30 Data Ready | MUX32 Addr 29 Data Ready | MUX32 Addr 28 Data Ready | MUX32 Addr 27 Data Ready | MUX32 Addr 26 Data Ready | MUX32 Addr 25 Data Ready | MUX32 Addr 24 Data Ready |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

### Acknowledge

The Acknowledge (Ack) bit will be set to one after the CM52 has detected a 1 in the Initiate bit of the Command Header. The CM52 will begin executing the command immediately following setting of the Acknowledge bit.

### Done

The (Command) Done bit will be set when the CM52 has completed the requested operation, has encountered an error condition, or the timeout value for the operation has expired. Timeout and Error conditions will be returned in bits 2 and 3.

### Timeout

Many commands set a Timeout period for the completion of a command. The Timeout value is expressed in 100 msec increments. If the Timeout value is set to 0, the CM52 will attempt to complete the operation until a Done or Error status is returned. When Timeouts are applied to serial operations, they control the amount of time permitted for each character.

In RFID operations, the Timeout applies to the time permitted for the transfer of each block of data to and from the tag. If the Timeout expires before the completion of the tag block transfer, the CM52 will set the Timeout bit and the Done bit to 1. When calculating the Timeout value, be sure to consider the amount of data being transferred, the Antenna transfer rate, and environmental conditions.

For example, an Antenna transfer rate of 3000 characters per second and a read or write of 600 characters would require a transfer time of approximately 200 ms. A Timeout value of 5 (representing 500 ms) would be appropriate for a 200 ms transfer. In noisy environments where data errors may occur, a longer Timeout is recommended to allow for retries.

### Error

The CM52 will set the Error bit to one if it encounters an incorrect parameter or command format. The Done bit will also be set.

### Digital Input

The Digital Inputs are used to indicate changes in the electrical state of the input points.

### Task Done

The Task Done bits are used to signal completion of Posted Commands. For example, you may post a "Read" to Antenna 0 using the Post Tag Read command. A response is given immediately by the CM52 acknowledging receipt of the request. When the Tag is completely read, that Tag's data is placed in the dedicated Task Buffer in the CM52 and the Task Done bit is set. After the Task Done bit is set, the buffered data may be transferred across the bus using the Buffer Read command. See page 89 for more information on Posted Commands.

### Data Ready

The following four bytes are the Data Ready flags, which represent a 32-bit array of the MUX32 bus. When a Slave device on the network has data for the PLC to retrieve, the MUX32 Data Ready bit corresponding to that Slave's multidrop address will be set to one. If your CM52 is configured as a 1/4 rack device, only the first 8 addresses (one byte) will be present in the response. All Data Ready bits will be present if the CM52 is configured as a 1/2 rack device.

### PLC Memory Mapping

The status and handshake Flags map directly to the PLC's input and output image files. The location of these bytes in PLC memory is determined by the CM52's Rack and Group address settings. The address of Word 0 will be I:RRG or O:RRG where RR is the Rack number and G is the Group number.

The tables below show how the Command and Response Flags map to the PLC I/O files for two examples of CM52 addresses: as a quarter-rack device at Rack 3, Group 0 and as a half-rack device at Rack 3, Group 2.

Bits are numbered in the charts below using octal notation.

Flag I/O addresses for quarter-rack CM52 starting at first quarter.

| **Discrete Output Data (Command Flags)** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | O:030/7 | O:030/6 | O:030/5 | O:030/4 | O:030/3 | O:030/2 | O:030/1 | O:030/0 |
| | MSB | O:030/17 | O:030/16 | O:030/15 | O:030/14 | O:030/13 | O:030/12 | O:030/11 | O:030/10 |
| Word 1 | LSB | O:031/7 | O:031/6 | O:031/5 | O:031/4 | O:031/3 | O:031/2<br>Dig Out 2 | O:031/1<br>Dig Out 1 | O:031/0<br>Init |
| | MSB | O:031/17 | O:031/16 | O:031/15 | O:031/14 | O:031/13 | O:031/12 | O:031/11 | O:031/10 |

| **Discrete Output Data (Response Flags)** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | I:030/7 | I:030/6 | I:030/5 | I:030/4 | I:030/3 | I:030/2 | I:030/1 | I:030/0 |
| | MSB | I:030/17 | I:030/16 | I:030/15 | I:030/14 | I:030/13<br>Task 3 Done | I:030/12<br>Task 2 Done | I:030/11<br>Task 1 Done | I:030/10<br>Task 0 Done |
| Word 1 | LSB | I:031/7 | I:031/6 | I:031/5<br>Dig In 2 | I:031/4<br>Dig In 1 | I:031/3<br>Error | I:031/2<br>Timeout | I:031/1<br>Done | I:031/0<br>Ack |
| | MSB | I:031/17<br>MUX32 Addr 07 Data Ready | I:031/16<br>MUX32 Addr 06 Data Ready | I:031/15<br>MUX32 Addr 05 Data Ready | I:031/14<br>MUX32 Addr 04 Data Ready | I:031/13<br>MUX32 Addr 03 Data Ready | I:031/12<br>MUX32 Addr 02 Data Ready | I:031/11<br>MUX32 Addr 01 Data Ready | I:031/10<br>MUX32 Addr 00 Data Ready |

Flag I/O addresses for half-rack CM52 starting at the second quarter.

| **Discrete Output Data (Command Flags)** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | O:032/7 | O:032/6 | O:032/5 | O:032/4 | O:032/3 | O:032/2 | O:032/1 | O:032/0 |
| | MSB | O:032/17 | O:032/16 | O:032/15 | O:032/14 | O:032/13 | O:032/12 | O:032/11 | O:032/10 |
| Word 1 | LSB | O:033/7 | O:033/6 | O:033/5 | O:033/4 | O:033/3 | O:033/2<br>Dig Out 2 | O:033/1<br>Dig Out 1 | O:033/0<br>Init |
| | MSB | O:033/17 | O:033/16 | O:033/15 | O:033/14 | O:033/13 | O:033/12 | O:033/11 | O:033/10 |
| Word 2 | LSB | O:034/7 | O:034/6 | O:034/5 | O:034/4 | O:034/3 | O:034/2 | O:034/1 | O:034/0 |
| | MSB | O:034/17 | O:034/16 | O:034/15 | O:034/14 | O:034/13 | O:034/12 | O:034/11 | O:034/10 |
| Word 3 | LSB | O:035/7 | O:035/6 | O:035/5 | O:035/4 | O:035/3 | O:035/2 | O:035/1 | O:035/0 |
| | MSB | O:035/17 | O:035/16 | O:035/15 | O:035/14 | O:035/13 | O:035/12 | O:035/11 | O:035/10 |

| Discrete Output Data (Command Flags) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | I:032/7 | I:032/6 | I:032/5 | I:032/4 | I:032/3 | I:032/2 | I:032/1 | I:032/0 |
| | MSB | I:032/17 | I:032/16 | I:032/15 | I:032/14 | I:032/13<br>Task 3 Done | I:032/12<br>Task 2 Done | I:032/11<br>Task 1 Done | I:032/10<br>Task 0 Done |
| Word 1 | LSB | I:033/7 | I:033/6 | I:033/5<br>Dig In 2 | I:033/4<br>Dig In 1 | I:033/3<br>Error | I:033/2<br>Timeout | I:033/1<br>Done | I:033/0<br>Ack |
| | MSB | I:033/17<br>MUX32 Addr 07 Data Ready | I:033/16<br>MUX32 Addr 06 Data Ready | I:033/15<br>MUX32 Addr 05 Data Ready | I:033/14<br>MUX32 Addr 04 Data Ready | I:033/13<br>MUX32 Addr 03 Data Ready | I:033/12<br>MUX32 Addr 02 Data Ready | I:033/11<br>MUX32 Addr 01 Data Ready | I:033/10<br>MUX32 Addr 00 Data Ready |
| Word 2 | LSB | I:034/7<br>MUX32 Addr 15 Data Ready | I:034/6<br>MUX32 Addr 14 Data Ready | I:034/5<br>MUX32 Addr 13 Data Ready | I:034/4<br>MUX32 Addr 12 Data Ready | I:034/3<br>MUX32 Addr 11 Data Ready | I:034/2<br>MUX32 Addr 10 Data Ready | I:034/1<br>MUX32 Addr 09 Data Ready | I:034/0<br>MUX32 Addr 08 Data Ready |
| | MSB | I:034/17<br>MUX32 Addr 23 Data Ready | I:034/16<br>MUX32 Addr 22 Data Ready | I:034/15<br>MUX32 Addr 21 Data Ready | I:034/14<br>MUX32 Addr 20 Data Ready | I:034/13<br>MUX32 Addr 19 Data Ready | I:034/12<br>MUX32 Addr 18 Data Ready | I:034/11<br>MUX32 Addr 17 Data Ready | I:034/10<br>MUX32 Addr 16 Data Ready |
| Word 3 | LSB | I:035/7<br>MUX32 Addr 31 Data Ready | I:035/6<br>MUX32 Addr 30 Data Ready | I:035/5<br>MUX32 Addr 29 Data Ready | I:035/4<br>MUX32 Addr 28 Data Ready | I:035/3<br>MUX32 Addr 27 Data Ready | I:035/2<br>MUX32 Addr 26 Data Ready | I:035/1<br>MUX32 Addr 25 Data Ready | I:035/0<br>MUX32 Addr 24 Data Ready |
| | MSB | I:035/17 | I:035/16 | I:035/15 | I:035/14 | I:035/13 | I:035/12 | I:035/11 | I:035/10 |

### 3.2.2 *Command and Response Parameters (Block Data)*

The ***parameter*** portion of the RF commands is transmitted using the PLC Block Transfer function. This is necessary because the number of data bytes required for an entire command and response exceeds the limited size of the discrete I/O buffers. The block data typically includes the command opcode, timeout value, data length, starting tag address, etc.

Block Transfers are limited to 64 words (128 bytes). Reads and writes of data lengths greater than 128 bytes will require multiple Block Transfers.

Block Transfer Reads may use a length of 0 – the CM52 will return the appropriate number of words for the command just executed. For instance, if a Tag Read command requesting 10 bytes from a tag is issued using a Block Transfer Write command, the subsequent Block Transfer Read command used to retrieve the data may request a length of 0 words. The CM52 will return 5 words of data because the previous command requested 10 bytes.

**Command Parameters**

The first word of the command parameter block data has the same format for all CM52 commands. The number and meaning of parameter / data words following the first word will vary with different commands. Refer to the individual command descriptions for information on remaining parameters.

The first command parameter word is defined as follows:

<table>
<tr><td rowspan="4">Word 0</td><td>MSB</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td></td><td colspan="8">OPCODE</td></tr>
<tr><td>LSB</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td></td><td colspan="5">Reserved</td><td colspan="2">Task Number<br><br>00 = Task 0<br>01 = Task 1<br>10 = Task 2<br>11 = Task 3</td><td>Device Number</td></tr>
</table>

**Opcode**
The first byte of the command parameters, the Opcode, tells the CM52 which operation it is to perform.

**Subopcode**
Following the Opcode is the Subopcode byte that specifies the Task Number (0-3) and the device being addressed (antenna or serial port).

**Device**
The ***device number*** refers to the RFID antenna or serial port that the command is addressing. The values can be:

0 = COM (Port) 1 or Antenna 0
1 = COM (Port) 2 or Antenna 1

**Task Number**
The CM52 has a multitasking operating system and up to four tasks may execute concurrently. The ***task number*** refers to the execution task assigned to the command and can have a value of 0-3 (binary 00-11) The task number should be set to 0 unless there are multiple tasks running concurrently.

**Response Parameters**
Many commands will have no block data response because the only CM52 response will be to set appropriate status bits in the Response Flags. Commands that cause data or additional status information to be returned by the CM52 will provide that data in response to a Block Transfer Read instruction. See the descriptions of the individual commands for the format of the block data returned.

## 3.3 Command Data Lengths

Since the Command and Response Flags are transferred in discrete data buffers, generally the entire Block Data buffer (up to 64 words, or 128 bytes) is available for data. However, certain commands contain other parameters within the block data that limit the number of data bytes.

The following table shows the amount of data that can be transferred in one Block Transfer operation for a sampling of CM52 commands.

**Table 13 — Maximum Transaction Size**

| CM52 Command | Maximum Data Bytes |
|---|---|
| HS Tag Write (one field) | 118 |
| HS Tag Write (two fields) | 114 |
| HS Tag Write (three fields) | 110 |
| HS Tag Read | 128 |
| Serial Write | 124 |
| Serial Read | 128 |
| HMS Tag Write (one field) | 118 |
| HMS Tag Write (two fields) | 114 |
| HS Tag Write (three fields) | 110 |
| HMS Tag Read | 128 |
| MUX32 Write | 58 |

Specific limitations are given in the command descriptions.

## 3.4 Block Transfer Problems

Unsolicited Block Transfers can occur if the first slot is used for discrete output data. In PLC-2 systems these problems can also result from input data assigned to the first slot. The first slot can not be used for input or output data in CM52 racks.

Problems may also occur with some scanners if a Block Transfer Read is requested when the scanner is requesting a Block Transfer Write or if a Block Transfer Write is requested when the scanner is requesting a Block Transfer Read.

## 3.5 Command Protocol

To issue a command, a sequence must be followed as shown in the flowchart below. The command parameters must first be downloaded using a Block Transfer Write command and then the Initiate bit should be set. The CM52 will immediately acknowledge receipt of the command by setting the Acknowledge bit to "1" and executing the command. When the PLC sees the Acknowledge bit set, it should reset the Initiate bit to 0. The CM52 will not set the Done bit until the command is completed and the transition from 1 to 0 is seen on the Initiate bit.

The flowchart in Figure 9 illustrates the handshake sequence for a Tag Write command.

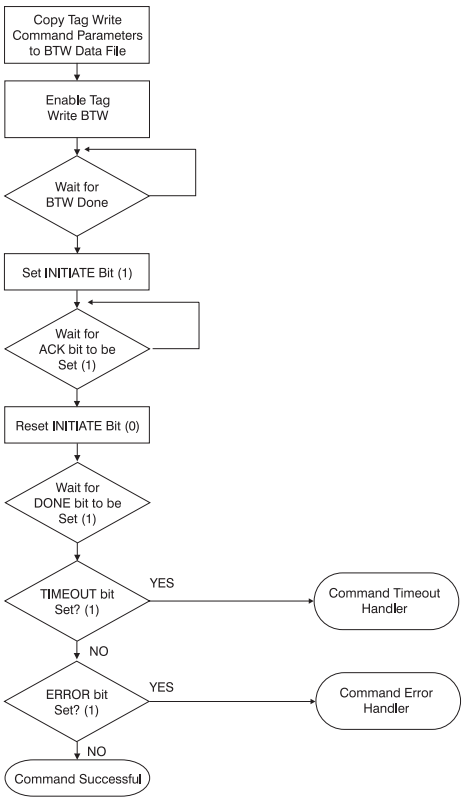


**Figure 9 — Tag Write Command Flow**

The flowchart in Figure 10 illustrates the handshake sequence for a Tag Read operation.

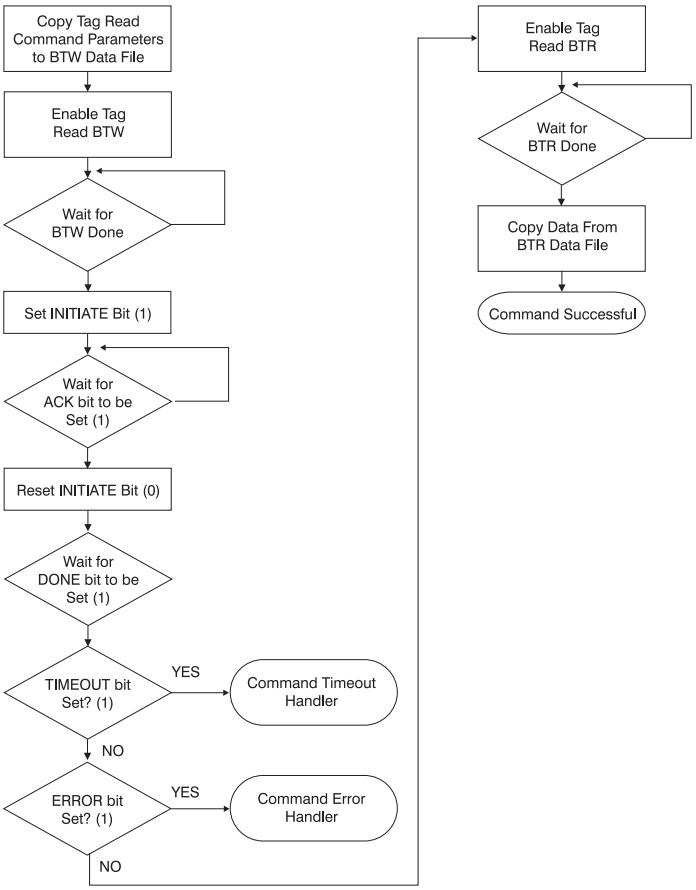


**Figure 10 — Tag Read Command Flow**

The sequences shown above demonstrate what is known as a 4-edge handshake and is the most secure method for message control. Execution of the command has begun while the second half of the handshake

is being negotiated. The overlap in processing is made possible by the real-time operating system and provides increased transaction speed.

Please refer to the product disk for example files written in both ladder logic and C language.

### *3.5.1 Posted Commands*

Posted Commands allow the Host to initiate multiple commands, and then receive acknowledgment from the CM52 while the commands are executing concurrently. A bit in the response Flags may be monitored to determine the status of the posted command.

After a Posted Read, a Buffer read must be performed to collect the data. Data for Posted Commands is read from, and written to, one of the four Task Buffers. After issuing a Buffer Write command, a Posted Write will complete the operation.

## 3.6 Command Descriptions

This section will provide details for each command supported by the CM52. For each command the following is given:

- A brief description of the command functionality
- The opcode and description of command parameters
- The order of parameters to be downloaded in the Block Transfer Write instruction
- A copy of the discrete bit maps for both the command and response flags
- The order of parameters to be uploaded in the Block Transfer Read instruction, where applicable
- The possible return status values

**NOTE:**
The Response Flags as shown are valid for a CM52 configured as a quarter-rack device. For half-rack configurations and additional three bytes of MUX32 Data Ready Flags would also be available.

Parameters are shown as words to match the integer fields of the PLC memory. The CM52 assumes data will be transmitted in the exact order as it appears in these descriptions.

Where a word is made up of two distinct one-byte parameters, the individual bytes will be identified. Where a byte contains bit-mapped fields, the individual bit values will be defined.

All offset and length parameters are given in bytes unless otherwise specified. Values are provided in decimal or hexadecimal format. Hexadecimal values are followed by an `H'. Bytes are read right to left with the least significant bit being 0.

Bit ordering in the discrete I/O blocks (command and response flags) are given in octal notation with the lower byte (LSB) first. Bit ordering in Transfer Blocks (parameters and data) is given in decimal with the upper byte (MSB) first.

Please see Appendix A for a command quick reference.

### 3.6.1 Initialization Commands

The following commands are typically executed once during initialization though they may be done at any time.

**Define Mode — Opcode 120**

Establish the mode for future commands.

Turning on ***Verify Mode*** causes all tag write commands to subsequently read the tag to verify that data was correctly stored. Turning on trace causes a trace of services executed to appear on serial port COM1. This is useful for debugging. Default is no verification and no trace. Enabling the time stamp causes a date-time stamp to appear in the trace.

***Swap Mode*** and ***Word Mode*** affect data being transferred by instructions such as tag read, tag write, serial read, etc. The explanation below illustrates transformations in hexadecimal. Only data transferred is affected. The instruction format remains the same.

Normally, the ***Define Mode*** command is not used since the default byte and word alignment is correct for the Allen-Bradley PLCs. This means, when transferring a string of bytes, the first byte, byte 0 is in the left-most half of the 16-bit register (upper byte), and byte 1 is in the right-most half (lower byte).

***Swap Mode***

The bytes are swapped in each word. i.e.,

| **Master** | | **Slave** |
|---|---|---|
| 1234 5678 | => | 3412 7856 (write) |
| 1234 5678 | <= | 3412 7856 (read) |

***Word Mode***

Words on the master are transformed to bytes on the slave. i.e.,

| **Master** | | **Slave** |
|---|---|---|
| 0012 0034 | => | 1234 (write) |
| 0012 0034 | <= | 1234 (read) |

***Swap Mode and Word Mode***

The bytes are swapped in each word. i.e.,

| **Master** | | **Slave** |
|---|---|---|
| 1200 3400 | => | 1234 (write) |
| 1200 3400 | <= | 1234 (read) |

Set up the Block Transfer Write data as follows.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 120 (78H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | | | |
| Word 1 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Reserved | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Word Mode 0=off 1=on | Swap Mode 0=off 0=on | Time Stamp 0=off 1=on | Ant. Type 0=HS 1=HL | Trace Mode 0=off 1=on | Tag Verify 0=off 1=on |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | |
| | MSB | Reserved | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### Define Serial Parameters — Opcode 10

Prior to doing serial I/O, the serial ports must be configured. Typically, this operation is only done once, during program initialization.

The default values are:

**COM1** = RS232 with a baud rate set at a value determined when the software is burned into EPROM. This is typically 9600 baud.

**COM2** = RS232, 9600, n, 8, 1

Set up the Block Transfer Write data as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 10 (0AH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | | | 0=COM1<br>1=COM2 |
| Word 1 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Reserved | | | | | | Data Bits<br>0=7<br>1=8 | Parity MSB<br>00=none<br>01=even<br>10=odd |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Parity LSB (see bit 8) | Stop Bits<br>0=1<br>1=2 | Baud Rate<br>0000 = 300<br>0001 = 600<br>0010 = 1200<br>0011 = 2400<br>0100 = 4800<br>0101 = 9600<br>0110 = 19200<br>0111 = 38400 | | | | Interface Type<br>00 = RS232<br>01 = RS422<br>10 = RS485<br>11 = RS485/ MUX32 | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | |
| | MSB | Reserved | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### 3.6.2 *Antenna Port Commands*

**HS Tag Fill — Opcode 4**

This command will fill a range or ranges of consecutive addresses in the active tag with a specified fill value. The maximum number of data bytes for a single field is 118, less 4 bytes for each additional field definition.

Set up the Block Transfer Write data as follows.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 4 (04H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=ANT0<br>1=ANT1 |
| Word 1 | MSB | Fill Byte (0-255) | | | | | | | |
| | LSB | Number of Fields to Follow (1-30) | | | | | | | |
| Word 2 | | Timeout Value (in 100 ms units, 0 = no timeout) | | | | | | | |
| Word 3 | | Field 1: Length (number of bytes) | | | | | | | |
| Word 4 | | Field 1: Start Address in RFID Tag | | | | | | | |
| Word 5 | | Field 2: Length (number of bytes) | | | | | | | |
| Word 6 | | Field 2: Start Address in RFID Tag | | | | | | | |
| Word (n x 2)+1 | | Field n: Length (number of bytes) | | | | | | | |
| Word (n x 2) +2 | | Field n: Start Address in RFID Tag | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | |
| | MSB | Reserved | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### HS Tag Read — Opcode 5

This command will read data from a range or ranges of consecutive addresses in the active tag into the CM52. The total number of data bytes for all fields cannot exceed 128 bytes in one tag read command. Multiple Tag Read commands or a Posted Tag Read command must be used if greater than 128 bytes of data must be read.

Once the command is Done, issue a Block Transfer Read instruction to retrieve the data from the CM52. The Block Transfer Read instruction may request a word length of 0 – the CM52 will return the number of bytes specified by the initial Tag Read command BTW.

Set up the Block Transfer Write data as follows.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 5 (05H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=ANT0<br>1=ANT1 |
| Word 1 | MSB | Reserved | | | | | | | |
| | LSB | Number of Fields to Follow (1-30) | | | | | | | |
| Word 2 | | Timeout Value (in 100 ms units, 0 = no timeout) | | | | | | | |
| Word 3 | | Field 1: Length (number of bytes) | | | | | | | |
| Word 4 | | Field 1: Start Address in RFID Tag | | | | | | | |
| Word 5 | | Field 2: Length (number of bytes) | | | | | | | |
| Word 6 | | Field 2: Start Address in RFID Tag | | | | | | | |
| Word (n x 2) +1 | | Field n: Length (number of bytes) | | | | | | | |
| Word (n x 2) + 2 | | Field n: Start Address in RFID Tag | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | |
| | MSB | Reserved | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

When the DONE flag is detected, issue a Block Transfer Read (BTR) to retrieve the data read from the Tag. The number of words requested can either be an exact number or if you use “0" the CM52 will return all the words retrieved from the last read command. The data will appear in the following format.

| | | |
|---|---|---|
| Word 0 | MSB | Data Byte 0 |
| | LSB | Data Byte 1 |
| Word 1 | MSB | Data Byte 2 |
| | LSB | Data Byte 3 |
| Word n | MSB | Data Byte (n x 2) |
| | LSB | Data Byte (n x 2) +1 |

### HS Tag Write — Opcode 6

This command will write data to a range or ranges of consecutive addresses in the active tag. The total number of data bytes for a single field cannot exceed 118 bytes in one tag read command. Subtract 4 bytes of data payload for each additional field definition. Multiple Tag Write commands or a Posted Tag Write command must be used if greater than 118 bytes of data must be written.

Set up the Block Transfer Write as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 6 (06H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=ANT0<br>1=ANT1 |
| Word 1 | MSB | Reserved | | | | | | | |
| | LSB | Number of Fields to Follow (1-24) | | | | | | | |
| Word 2 | | Timeout Value (in 100 ms units, 0 = no timeout) | | | | | | | |
| Word 3 | | Field 1: Length (number of bytes) | | | | | | | |
| Word 4 | | Field 1: Start Address in RFID Tag | | | | | | | |
| Word 5 | | Field 2: Length (number of bytes) | | | | | | | |
| Word 6 | | Field 2: Start Address in RFID Tag | | | | | | | |
| Word (n x 2) +1 | | Field n: Length (number of bytes) | | | | | | | |
| Word (n x 2) +2 | | Field n: Start Address in RFID Tag | | | | | | | |
| Word (F x 2) + 3 | | Words with the data to be written where "F" is the number of fields. Byte 0 is the MSB followed by byte 1 as LSB and so forth. | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### Reset Tag Battery Timer — Opcode 13

Resets the Battery Timer in the tag (in the range of the specified antenna).

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 13 (0DH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0 = ANT0<br>1 = ANT1 |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### Tag-to-Tag Transfer — Opcode 20

Copies data from one Tag Memory area to another Tag Memory area.

This command can be used to copy data from one location in a Tag to another location in the same Tag, or to copy data from an area of one tag to an area of the other Tag. Either of the two HS antennas can be designated as the Read and Write Antenna. If Tag Verify is enabled, the data written to the Write Antenna is read back and verified.

The Timeout parameter applies to the read and write operations (and the verify operation, if enabled) individually, not the entire transfer operation.

The command returns upon completion, or when an error or timeout is encountered in any one of the nested operations. Therefore, status returned can indicate an error or timeout condition in the read, write or verify operations.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 20 (14H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Read Antenna (0 or 1) | | | | | | | |
| | LSB | Write Antenna (0 or 1) | | | | | | | |
| Word 2 | | Starting Tag Address to read from, in bytes | | | | | | | |
| Word 3 | | Starting Tag Address to write to, in bytes | | | | | | | |
| Word 4 | | Number of bytes to transfer | | | | | | | |
| Word 5 | | Timeout - in 100 ms units, 0 = no timeout | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### *3.6.3 RS232 Serial Interface Commands*

RS232 Serial Interface commands are divided into two groups - General and HMS-specific. These are explained in the following two sub-sections.

**General RS232 Commands**

NOTE: The maximum length per command is limited to 126 bytes by the maximum 128 less 2 bytes of overhead. The serial port circular buffers are 1 kbyte. For longer reads or writes, use the Post Serial Read/Write commands.

**Serial ReadLn — Opcode 9**

Reads a specified length of data from a selected serial port. Data is read until the maximum read length is reached, or the termination character is found.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 9 (09H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=COM1<br>1=COM2 |
| Word 1 | | Timeout Value (given in 100 ms units, 0 = no timeout) | | | | | | | |
| Word 2 | MSB | Termination Character (user selected) | | | | | | | |
| | LSB | Number of bytes to read. 1-126 (binary 0000 0001 = 1 byte, etc.) | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

When the DONE flag is detected, issue a Block Transfer Read (BTR) to retrieve the data read from the Tag. The number of words requested can either be an exact number or if you use “0" the CM52 will return all the words retrieved from the last read command. The data will appear in the following format with the first word used for overhead.

| | | |
|---|---|---|
| Word 0 | MSB | Reserved |
| | LSB | Number of bytes read |
| Word 1 | MSB | Data byte 0 |
| | LSB | Data byte 1 - continued until the end of the data field |
| Word n | MSB | Data byte (n x 2) |
| | LSB | Data byte (n x 2) + 1 |

### Serial Read — Opcode 11

Reads up to 128 characters of data from the specified serial port.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 11 (0BH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=COM1<br>1=COM2 |
| Word 1 | | Timeout Value (given in 100 ms units, 0 = no timeout) | | | | | | | |
| Word 2 | MSB | Reserved | | | | | | | |
| | LSB | Number of bytes to read (binary 0000 0001 = 1 byte, etc.) | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

When the DONE flag is detected, issue a Block Transfer Read (BTR) to retrieve the data read from the Tag. The number of words requested can either be an exact number or if you use “0" the CM52 will return all the words retrieved from the last read command. The data will appear in the following format.

| | | |
|---|---|---|
| Word 0 | MSB | Data Byte 0 |
| | LSB | Data Byte 1 |
| Word 1 | MSB | Data Byte 2 |
| | LSB | Data Byte 3 |
| Word n | MSB | Data Byte (n x 2) |
| | LSB | Data Byte (n x 2) +1 |

### Serial Write — Opcode 12

Writes up to 124 bytes of data to the specified serial port.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 12 (0CH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=COM1<br>1=COM2 |
| Word 1 | MSB | Reserved | | | | | | | |
| | LSB | Number of bytes to write, 1-124 bytes (binary 0000 0001 = 1 byte, etc.) | | | | | | | |
| Word 2 | MSB | Data byte 0 | | | | | | | |
| | LSB | Data byte 1 | | | | | | | |
| Word 3 | MSB | Data byte 2 | | | | | | | |
| | LSB | Data byte 3 - until the end of the data to be written. | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### Clear Serial Buffers — Opcode 14

Clears the Input/Output Serial Buffers for the designated serial port.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 14 (0EH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=COM1<br>1=COM2 |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

## HMS Tag Fill (RS232) — Opcode 16

Writes a fill byte to consecutive HMS tag address at the specified serial port. You can define as many as 30 different fill fields.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 16 (10H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=COM1<br>1=COM2 |
| Word 1 | MSB | Fill Byte (0-255) | | | | | | | |
| | LSB | Number of Fields to Follow (1-30) | | | | | | | |
| Word 2 | | Timeout Value (in 100 ms units, 0 = no timeout) | | | | | | | |
| Word 3 | | Field 1: Length (number of bytes) | | | | | | | |
| Word 4 | | Field 1: Start Address in RFID Tag | | | | | | | |
| Word 5 | | Field 2: Length (number of bytes) | | | | | | | |
| Word 6 | | Field 2: Start Address in RFID Tag | | | | | | | |
| Word (n x 2) +1 | | Field n: Length (number of bytes) | | | | | | | |
| Word (n x 2) +2 | | Field n: Start Address in RFID Tag | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | |
| | MSB | Reserved | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### HMS Tag Read (RS232) — Opcode 17

Reads data from the HMS Tag at the specified serial port. The total number of data bytes for all fields is 128.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 17 (11H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=COM1<br>1=COM2 |
| Word 1 | MSB | Reserved | | | | | | | |
| | LSB | Number of Fields to Follow (1-24) | | | | | | | |
| Word 2 | | Timeout Value (in 100 ms units, 0 = no timeout) | | | | | | | |
| Word 3 | | Field 1: Length (number of bytes) | | | | | | | |
| Word 4 | | Field 1: Start Address in RFID Tag | | | | | | | |
| Word 5 | | Field 2: Length (number of bytes) | | | | | | | |
| Word 6 | | Field 2: Start Address in RFID Tag | | | | | | | |
| Word (n x 2) + 1 | | Field n: Length (number of bytes) | | | | | | | |
| Word (n x 2) + 2 | | Field n: Start Address in RFID Tag | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

When the DONE flag is detected, issue a Block Transfer Read (BTR) to retrieve the data read from the Tag. The number of words requested can either be an exact number or if you use “0" the CM52 will return all the words retrieved from the last read command. The data will appear in the following format. A maximum of 128 bytes of data can be retrieved.

| | | |
|---|---|---|
| Word 0 | MSB | Data Byte 0 |
| | LSB | Data Byte 1 |
| Word 1 | MSB | Data Byte 2 |
| | LSB | Data Byte 3 |
| Word n | MSB | Data Byte (n x 2) |
| | LSB | Data Byte (n x 2) +1 |

### HMS Tag Write (RS232) — Opcode 18

Writes data to the HMS Tag at the specified serial port. A maximum of 118 bytes can be written using a single field. Reduce the data payload by 2 bytes for each additional field definition.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 18 (12H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=COM1<br>1=COM2 |
| Word 1 | MSB | Reserved | | | | | | | |
| | LSB | Number of Fields to Follow (1-11) | | | | | | | |
| Word 2 | | Timeout Value (in 100 ms units, 0 = no timeout) | | | | | | | |
| Word 3 | | Field 1: Length (number of bytes) | | | | | | | |
| Word 4 | | Field 1: Start Address in RFID Tag | | | | | | | |
| Word 5 | | Field 2: Length (number of bytes) | | | | | | | |
| Word 6 | | Field 2: Start Address in RFID Tag | | | | | | | |
| Word (n x 2) + 1 | | Field n: Length (number of bytes) | | | | | | | |
| Word (n x 2) + 2 | | Field n: Start Address in RFID Tag | | | | | | | |
| Word (F x 2) + 3 | | Data bytes to write, where "F" is the field number (118 bytes max.) | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### *3.6.4 MUX32 Serial Interface Commands*

These commands allow specification of which device on the MUX32 multidrop to read or write. When a device on the network has a response ready, it sets the corresponding bit in the Data Ready word of the Response Header. Use the Collect command (Opcode 39) for Read commands (only) to retrieve the data from the device. The Data Ready words may have more than one bit set at a time, indicating multiple devices are ready with responses.

The MUX32 Serial Interface commands are divided into four groups - General , HMS, General Auto-polled, and HMS Auto-polled. They are explained in the following sub-sections.

**General MUX32 Commands**

**MUX32 Read — Opcode 30**

Instructs the CM52 to read data from the specified MUX32 slave. A Collect command should be issued via a BTW, to retrieve the data and status once the corresponding Data Ready bit is detected in the response header.

The Block Write Transfer is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 30 (1EH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Reserved | | | | | | | |
| | LSB | MUX32 Address of Slave device | | | | | | | |
| Word 2 | | Timeout Value (given in 100 ms units, 0 = no timeout) | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### MUX32 Write — Opcode 31

Writes up to 124 bytes of data to the specified MUX32 slave.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 31 (1FH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Length of data in bytes | | | | | | | |
| | LSB | MUX32 Address of Slave device | | | | | | | |
| Word 2 | MSB | Data byte 0 | | | | | | | |
| | LSB | Data byte 1 | | | | | | | |
| Word 3 | MSB | Data byte 2 | | | | | | | |
| | LSB | Data byte 3 etc... (124 bytes max.) | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### MUX32 Collect — Opcode 39

This command should be issued to a Slave when its Data ready bit is set. The Collect command resets the Data Ready bit and returns status and data for the previously issued 30-series command.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 39 (27H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Reserved | | | | | | | |
| | LSB | MUX32 Address of Slave device | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

When the DONE flag is detected, issue a Block Transfer Read (BTR) to retrieve the data read from the Tag. The number of words requested can either be an exact number or if you use “0" the CM52 will return all the words retrieved from the last read command. The data will appear in the following format with the first word used for overhead.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Reserved | | | | Error | Timeout | Done | Reserved |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Length of data in bytes | | | | | | | |
| Word 1 | MSB | Data byte 0 | | | | | | | |
| | LSB | Data byte 1 | | | | | | | |
| Word n | MSB | Data byte (n x 2) | | | | | | | |
| | LSB | Data byte (n x 2) + 1 | | | | | | | |

## HMS MUX32 Tag Read — Opcode 32

Reads data from the HMS Tag (in range of the specified antenna) over the MUX32 bus. Control is returned immediately. When the Slave's Data Ready bit is set, issue a Collect command (Opcode 39) to retrieve status and data.

The Block Transfer Write data is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 32 (20H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Length of data in bytes | | | | | | | |
| | LSB | MUX32 Address of Slave device | | | | | | | |
| Word 2 | | Start address in RFID tag | | | | | | | |
| Word 3 | | Timeout Value (given in 100 ms units, 0 = no timeout) | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### HMS MUX32 Tag Write — Opcode 33

Writes up to 58 bytes of data to the HMS tag in range of the specified antenna. Control is returned immediately. When the Slave's Data Ready Bit is set, issue a Collect command (Opcode 39) to retrieve status.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 33 (21H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Length of data in bytes. 1-58 bytes | | | | | | | |
| | LSB | MUX32 Address of Slave device | | | | | | | |
| Word 2 | | Start address in RFID tag | | | | | | | |
| Word 3 | | Timeout Value (given in 100 ms units, 0 = no timeout) | | | | | | | |
| Word 4 | | Data byte 0 | | | | | | | |
| Word 5 | | Data byte 1 | | | | | | | |
| Word n | | Data byte 2 etc. | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### HMS MUX32 Tag Fill — Opcode 34

Writes a fill byte to consecutive addresses in the HMS Tag (in range of the specified antenna). When the Slave's Data Ready bit is set, issue a Collect command (Opcode 39) to retrieve status and data.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 34 (22H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Fill byte | | | | | | | |
| | LSB | MUX32 Address of Slave device | | | | | | | |
| Word 2 | | Length of fill in bytes | | | | | | | |
| Word 3 | | Start address in RFID tag | | | | | | | |
| Word 4 | | Timeout Value (given in 100 ms units, 0 = no timeout) | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 R–eady | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### 3.6.5 General Auto-Polled MUX32 Commands

The 40-series Auto-polled MUX32 Read command (opcode 40) polls the entire bus and returns data from the next active device that has data.

The 40-Series commands are not compatible and cannot be used in conjunction with 30-Series commands.

A Data Ready bit is set in the response from a Read command indicating which device responded, and that the data has been returned. The Data Ready bit is automatically reset by the next Read command issued. The address of the responding device is included in the response message packet with the status of the previously issued MUX32 command.

The MUX32 Read command is used in conjunction with the 40-series HMS antenna commands (Read, Write, and Fill) to collect status and data from specified MUX32 slaves; since those commands only post the requested operation, then return immediately.

In typical applications, the auto-polled MUX32 Read command would continuously poll the bus while other operations, such as an HMS Tag Read or Write, execute concurrently.

Only one Data Ready bit is set at a time using the 40-Series commands.

### MUX32 Read (Auto-polled) — Opcode 40

Polls the MUX32 bus and returns either when data is received from a responding slave; or when the timeout period expires with no slaves responding.

The status and address of the responding slave and the number of bytes returned are included in the response along with the data itself. Two status bytes are returned:

- The standard response header status indicates status of the Read command itself.
- The status returned in the BTR response byte 0, indicates MUX32 status of the previously issued command.

The command is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 40 (28H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | | Timeout, in 100 ms units. 0 = no timeout | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

When the DONE flag is detected, issue a Block Transfer Read (BTR) to retrieve the data read from the Tag. The number of words requested can either be an exact number or if you use “0" the CM52 will return all the words retrieved from the last read command. The data will appear in the following format with the first two words used for overhead.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Reserved | | | | Error | Timeout | Done | Reserved |
| | LSB | Responding Slave Address | | | | | | | |
| Word 1 | MSB | Length of data in bytes | | | | | | | |
| | LSB | Data byte 0 | | | | | | | |
| Word 2 | MSB | Data byte 1 | | | | | | | |
| | LSB | Data byte 2 | | | | | | | |
| Word 3 | MSB | Data byte 3 | | | | | | | |
| | LSB | Data byte 4 etc. | | | | | | | |

### MUX32 Write (Auto-Polled) — Opcode 41

Writes up to 58 byte of data to the specified MUX32 slave.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 41 (29H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Length of data in bytes, 1-58 bytes | | | | | | | |
| | LSB | MUX32 Address | | | | | | | |
| Word 2 | MSB | Data byte 0 | | | | | | | |
| | LSB | Data byte 1 | | | | | | | |
| Word 3 | MSB | Data byte 2 | | | | | | | |
| | LSB | Data byte 3 etc... | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | |
| | MSB | Reserved | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

## HMS MUX32 Tag Read (Auto-Polled) — Opcode 42

Reads data from the HMS Tag at the antenna specified. Control is returned immediately. The MUX32 command (Opcode 40) should be issued following the Tag read command to retrieve the data and status of the read operation.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 42 (2AH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Length of data in bytes | | | | | | | |
| | LSB | MUX32 Address | | | | | | | |
| Word 2 | | Start Address in Tag | | | | | | | |
| Word 3 | | Timeout Value (given in 100 ms units, 0 = no timeout) | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### HMS MUX32 Tag Write (Auto-Polled) — Opcode 43

Write up to 58 bytes of data to the HMS Tag at the Antenna specified. Control is returned immediately. The MUX32 Read command (Opcode 43) should be issued following the Tag Write Command to retrieve the status of the Write operation.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 43 (29H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Length of data in bytes, 1-58 bytes | | | | | | | |
| | LSB | MUX32 Address | | | | | | | |
| Word 2 | | Start Address in Tag | | | | | | | |
| Word 3 | | Timeout Value (given in 100 ms units. 0 = no timeout) | | | | | | | |
| Word 4 | MSB | Data byte 0 | | | | | | | |
| | LSB | Data byte 1 | | | | | | | |
| Word n | MSB | Data byte 2 | | | | | | | |
| | LSB | Data byte 3, etc. | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### HMS MUX32 Tag Fill (Auto-polled) — Opcode 44

A Fill Byte is written to consecutive addresses in the HMS Tag at the Antenna specified. Control is returned immediately. The MUX32 Read Command (Opcode 40) should be issued following the Tag Fill to retrieve the status of the fill operation.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 44 (2CH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Fill byte | | | | | | | |
| | LSB | MUX32 Address | | | | | | | |
| Word 2 | | Length of fill in bytes | | | | | | | |
| Word 3 | | Start address in Tag | | | | | | | |
| Word 4 | | Timeout Value (given in 100 ms units. 0 = no timeout) | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error or Timeout) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Timeout | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### 3.6.6 *Posted Commands*

Posted commands separate the request for an operation (execution of a posted command) from the transfer of data (completion of a task). This separation permits the CM52 to process up to four requested operations simultaneously.

After a posted command has been requested, the CM52 responds immediately, confirming the command before actually transferring data. When the second stage of the operation is complete, the Task Done bit is set in the Response Flags, indicating that data and status information is ready for retrieval from the Task Buffer. Data for posted commands is transferred through one of four Task Buffers. The Task Buffers have a maximum of 16,384 bytes each.

There are two types of posted commands, Read commands and Write commands:

**Read Commands**

On receipt of a "Read" posting command, the CM52 does the following:

- The Task Done bit is cleared.
- The CM52 completes the handshake protocol as described on page , and returns a Done in the Response Header.
- The data is read from the tag or serial port.
- The data is stored in a Task Buffer in the CM52.
- The Task Done bit is set when the operation is complete.

The host PLC should take the following actions:

- On receipt of a posted Read Done from the CM52, begin monitoring the Task Done bit.
- When the Task Done bit is set, use the Buffer Read Command to retrieve the status and data of the posted command.

- Continue reading until the Buffer Read command returns a length of 0. Each successive call will retrieve the next segment in the Task Buffer.

### Write Commands

Prior to invoking a posted write, the data to be written must be moved to the Task Buffer using one or more Buffer Write commands. Repeat the Buffer Write command until all data is written to the Task Buffer. Each successive call will append the data to the next segment in the Task Buffer.

On receipt of the "Write" posting command, the CM52 does the following:

- Clears the Task Done bit.
- Completes the handshake protocol as described on page , and returns a Done in the Response Header.
- Writes the data to the tag or serial port using data in the Task Buffer.
- When the operation is complete, clears the Task Buffer of write data and then writes status data.
- Sets the Task Done bit.

The host PLC should take the following actions:

- On receipt of a posted Write Done from the CM52, begin monitoring the Task Done bit.
- When the Task Done bit is set, use the Buffer Read Command to determine the status of the posted command.

### Post Tag Read — Opcode 60

A Tag Read is posted. Reads Data from the Tag in range of the specified antenna.

The Block Transfer Write is formatted as follows.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 60 (3CH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=ANT0<br>1=ANT1 |
| Word 1 | MSB | Reserved | | | | | | | |
| | LSB | Number of Fields to Follow (1-24) | | | | | | | |
| Word 2 | | Timeout Value (in 100 ms units, 0 = no timeout) | | | | | | | |
| Word 3 | | Field 1: Length (number of bytes) | | | | | | | |
| Word 4 | | Field 1: Start Address in RFID Tag | | | | | | | |
| Word 5 | | Field 2: Length (number of bytes) | | | | | | | |
| Word 6 | | Field 2: Start Address in RFID Tag | | | | | | | |
| Word (n x 2) + 1 | | Field n: Length (number of bytes) | | | | | | | |
| Word (n x 2) + 2 | | Field n: Start Address in RFID Tag | | | | | | | |

When the command BTW is complete set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### Post Tag Write — Opcode 61

A Tag Write is posted. Writes data to the tag in range of the specified antenna. The total number of data bytes for a single field cannot exceed 118 bytes in one tag read command. Subtract 4 bytes of data payload for each additional field definition

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 61 (3DH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0 = ANT0<br>1 = ANT1 |
| Word 1 | MSB | Reserved | | | | | | | |
| | LSB | Number of Fields to Follow (1-24) | | | | | | | |
| Word 2 | | Timeout Value (in 100 ms units, 0 = no timeout) | | | | | | | |
| Word 3 | | Field 1: Length (number of bytes) | | | | | | | |
| Word 4 | | Field 1: Start Address in RFID Tag | | | | | | | |
| Word 5 | | Field 2: Length (number of bytes) | | | | | | | |
| Word 6 | | Field 2: Start Address in RFID Tag | | | | | | | |
| Word (n x 2) + 1 | | Field n: Length (number of bytes) | | | | | | | |
| Word (n x 2) + 2 | | Field n: Start Address in RFID Tag | | | | | | | |
| Word (F x 2) + 3 | | Data bytes to write, where "F" is the field number (118 bytes max.) | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### Post Serial Read — Opcode 62

A Serial Read command is posted. Reads data from the specified serial port.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 62 (3EH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=COM1<br>1=COM2 |
| Word 1 | MSB | Timeout Value (given in 100 ms units, 0= no timeout) | | | | | | | |
| | LSB | Length of read in bytes | | | | | | | |
| Word 2 | | Start address in RFID tag | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

### Post Serial ReadLn — Opcode 63

A Serial ReadLn is posted. Reads data from a specified serial port. Data is read until the maximum read length is reached or the termination character is found.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 63 (3FH) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | 0=COM1<br>1=COM2 |
| Word 1 | MSB | Timeout Value (given in 100 ms units, 0 = no timeout) | | | | | | | |
| | LSB | Length of read in bytes | | | | | | | |
| Word 2 | MSB | Reserved | | | | | | | |
| | LSB | Termination Character | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

**Buffer Read — Opcode 68**

Reads data from the Task Buffer designated by the Task Number. Issue this command using the same Task Number as the Posted Command, (only) after the Task Done bit is set. The first call to Buffer Read following a Posted Read retrieves data starting at buffer offset 0. Subsequent calls step through the buffer, retrieving additional data. The buffer size for each task is 16,384 bytes. If no data remains, the read operation returns a positive confirmation with a length of 0.

The Block Transfer Write is formatted as follows:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 68 (44H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

**Response —Posted Write**

The Posted Write Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

When the DONE flag is detected, issue a Block Transfer Read (BTR) to retrieve the data read from the Tag. The number of words requested can either be an exact number or if you use “0" the CM52 will return all the words retrieved from the last read command. The status will appear in the following format with the first word used for overhead.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | Reserved | | | | Error | Timeout | Done | Reserved |
| | LSB | Reserved | | | | | | | |

**Response —Posted Read**

The Posted Read Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

To retrieve the data read from the Tag you must issue a Block Transfer Read (BTR) to collect the command status and data from the CM52. Up to 126 bytes of data can be returned.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | Error | Timeout | Done | Reserved |
| | LSB | Length of data in bytes, 1- 126 bytes | | | | | | | |
| Word 1 | MSB | Data byte 0 | | | | | | | |
| | LSB | Data byte 1 | | | | | | | |
| Word 2 | MSB | Data byte 2 | | | | | | | |
| | LSB | Data byte 3 etc. | | | | | | | |

### Buffer Write — Opcode 69

Writes data to the Task Buffer designated. Issue the subsequent Posted Write command using the Task Number as the Buffer Write Command. The first call to Buffer Write is done at buffer offset 0. Subsequent writes are appended to the buffer. When a Posted Write is done, the buffer is cleared, and the next call to Buffer Write will place data at buffer offset 0. The buffer size for each task is 16,384 bytes.

To retrieve the status of the original posted command, issue a Buffer Read Command. Up to 124 bytes of data can be written.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | OPCODE 69 (45H) | | | | | | | |
| | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Task Number | | Reserved |
| Word 1 | MSB | Reserved | | | | | | | |
| | LSB | Number of bytes to write | | | | | | | |
| Word 2 | MSB | Data byte 0 | | | | | | | |
| | LSB | Data byte 1 | | | | | | | |
| Word n | MSB | Data byte 2 | | | | | | | |
| | LSB | Data byte 3 etc. | | | | | | | |

When the command BTW is complete, set the Initiate bit in the output file.

The Command Flags bit map is shown below. The address of Word 0 is O:rrg where O indicates the output file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | Used by scanner for block transfers | | | | | | | |
| | MSB | Reserved | | | | | | | |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | | | | Digital Out 2 | Digital Out 1 | Initiate |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | | | | |

The CM52 will respond by setting the Ack flag when it sees the Initiate flag to signal receipt of the command buffer. When the command is completed the CM52 will set the Done (and possibly Error) flag in the Input file.

The Response Flags bit map is shown below. The address of Word 0 is I:rrg where I indicates the input file, rr is the CM52 rack address and g is the CM52 group assignment.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Word 0 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Used by scanner for block transfers | | | | | | | |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | Reserved | | | | Task 3 Done | Task 2 Done | Task 1 Done | Task 0 Done |
| Word 1 | LSB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | Digital In 2 | Digital In 1 | Error | Reserved | Done | Ack |
| | MSB | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| | | MUX32 Addr 07 Ready | MUX32 Addr 06 Ready | MUX32 Addr 05 Ready | MUX32 Addr 04 Ready | MUX32 Addr 03 Ready | MUX32 Addr 02 Ready | MUX32 Addr 01 Ready | MUX32 Addr 00 Ready |

If the CM52 is configured as a 1/2 rack device, the remaining MUX32 status bits will be present in word 2 and word 3.

# A APPENDIX QUICK REFERENCE

| Command | Opcode | | | Description | Page |
|---|---|---|---|---|---|
| | Decimal | Binary | Hex | | |
| Tag Fill | 4 | 0000 0100 | 04 | Fill tag with repeating byte | 38 |
| Tag Read | 5 | 0000 0101 | 05 | Read tag at RFID port | 40 |
| Tag Write | 6 | 0000 0110 | 06 | Write to tag at RFID port | 43 |
| Serial ReadLn (RS232) | 9 | 0000 1001 | 09 | Read serial data until termination character | 49 |
| Define Serial Parameters | 10 | 0000 1010 | 0A | Sets serial interfaces | 36 |
| Serial Read (RS232) | 11 | 0000 1011 | 0B | Read data from serial port | 52 |
| Serial Write (RS232) | 12 | 0000 1100 | 0C | Write data to serial port | 54 |
| Reset Tag Battery Timer | 13 | 0000 1101 | 0D | Battery time byte on tag is cleared | 45 |
| Clear Serial Buffers | 14 | 0000 1110 | 0E | Clears input/output serial buffers | 56 |
| HMS Tag Fill (RS232) | 16 | 0001 0000 | 10 | Fills tags with repeated byte | 58 |
| HMS Tag Read (RS232) | 17 | 0001 0001 | 11 | Read HMS tag at RFID port | 60 |
| HMS Tag Write (RS232) | 18 | 0001 0010 | 12 | Write to tag at RFID port | 63 |
| Tag-to-Tag Transfer | 20 | 0001 0100 | 14 | Copies data from one tag to another | 47 |
| Serial Read (MUX32) | 30 | 0001 1110 | 1E | Read data from MUX32 slave | 65 |
| Serial Write (MUX32) | 31 | 0001 1111 | 1F | Write data to MUX32 slave | 67 |
| HMS Tag Read (MUX32) | 32 | 0010 0000 | 20 | Read data to HMS tag via MUX32 slave | 71 |
| HMS Tag Write (MUX32) | 33 | 0010 0001 | 21 | Write data to HMS tag via MUX32 slave | 73 |
| HMS Tag Fill (MUX32) | 34 | 0010 0010 | 22 | Fills HMS tag with repeated byte via MUX32 slave | 75 |
| Collect (MUX32) | 39 | 0010 0111 | 27 | Retrieves data from 30-Series commands | 69 |
| Read, Auto-polled (MUX32) | 40 | 0010 1000 | 28 | Polls MUX32 Bus, returns data, status, and address of responding slave | 88 |
| Write, Auto-polled (MUX32) | 41 | 0010 1001 | 29 | Writes data to specified MUX32 slave | 91 |

| Command | Opcode | | | Description | Page |
|---|---|---|---|---|---|
| | Decimal | Binary | Hex | | |
| Tag Read, Auto-polled (HMS MUX32) | 42 | 0010 1010 | 2A | Reads data from HMS Tag at specified Antenna | 83 |
| Tag Writ, Auto-polled (HMS MUX32) | 43 | 0010 1011 | 2B | Writes data to HMS Tag at specified Antenna | 85 |
| Tag Fill,Auto-polled (HMS MUX32) | 44 | 0010 1100 | 2C | Writes Fill Byte to addresses in HMS Tag at specified Antenna | 87 |
| Post Tag Read | 60 | 0011 1100 | 3C | Tag read is posted | 91 |
| Post Tag Write | 61 | 0011 1101 | 3D | Tag write is posted | 93 |
| Post Serial Read | 62 | 0011 1110 | 3E | Serial read is posted | 95 |
| Post Serial ReadLn | 63 | 0011 1111 | 3F | Serial ReadLn is Posted | 97 |
| Buffer Read | 68 | 0100 0100 | 44 | Reads data from Task Buffer following posted command | 99 |
| Buffer Write | 69 | 0100 0101 | 45 | Write data to Task Buffer preceding a posted write command | 102 |
| Define Mode | 120 | 0111 1000 | 78 | Establishes global parameters | 32 |

# B APPENDIX SPECIFICATIONS

| | |
|---|---|
| Electrical | |
| Supply Voltage | 24 VDC (+/-15%) |
| Current Consumption | 350 mA (module only)<br>900 mA (with antennas) |
| Communication | |
| Compatibility | Remote I/O |
| RFID Interface | Two HS/HL-Series antenna ports<br>HMS-Series through serial ports |
| COM1 | RS232 |
| COM2 | RS232/RS422/RS485 (MUX32) |
| Inputs - CM52 | Two industrial-level inputs, 10-30 Vdc |
| Output - CM52 | Two industrial-level output, 5-30 Vdc<br>(400 mA, sinking) |
| Mechanical Specifications | |
| Dimensions (L x W x H) | 2.00 x 7.50 x 6.00 inches<br>(51 x 191x 152 cm) |
| Weight | 2.0 lb. (0.9 kg) |
| Enclosure | EMI shielded ABS shell |
| **Environmental** | |
| Operating Temperature | +32 to 122 degrees F<br>(0 to 50 degrees C) |
| Storage Temperature | -4 to 158 degrees F<br>(-20 to 70 degrees C) |
| Humidity | 90% non-condensing |
| Shock Resistance | IEC 68-2-27 test EA 30g;<br>11 msec; 3 shocks each axis |
| Vibration Resistance | IEC 68-2-6 test FC 1.5 mm;<br>10 to 55 Hz; 2 hours each axis |
| Protection Class | NEMA 2 (IP31) |

**NOTE**:Specifications are subject to change without notice.

# C APPENDIX ASCII CHART

| Decimal | Hex | Character | Decimal | Hex | Character |
|---|---|---|---|---|---|
| 000 | 00 | NUL | 030 | 1E | RS |
| 001 | 01 | SOH | 031 | 1F | US |
| 002 | 02 | STX | 032 | 20 | (space) |
| 003 | 03 | ETX | 033 | 21 | ! |
| 004 | 04 | EOT | 034 | 22 | " |
| 005 | 05 | ENQ | 035 | 23 | # |
| 006 | 06 | ACK | 036 | 24 | $ |
| 007 | 07 | BEL | 037 | 25 | % |
| 008 | 08 | BS | 038 | 26 | & |
| 009 | 09 | HT | 039 | 27 | ` |
| 010 | 0A | LF | 040 | 28 | ( |
| 011 | 0B | VT | 041 | 29 | ) |
| 012 | 0C | FF | 042 | 2A | * |
| 013 | 0D | CR | 043 | 2B | + |
| 014 | 0E | SO | 044 | 2C | ' |
| 015 | 0F | SI | 045 | 2D | - |
| 016 | 10 | DLE | 046 | 2E | . |
| 017 | 11 | DC1 | 047 | 2F | / |
| 018 | 12 | DC2 | 048 | 30 | 0 |
| 019 | 13 | DC3 | 049 | 31 | 1 |
| 020 | 14 | DC4 | 050 | 32 | 2 |
| 021 | 15 | NAK | 051 | 33 | 3 |
| 022 | 16 | SYN | 052 | 34 | 4 |
| 023 | 17 | ETB | 053 | 35 | 5 |
| 024 | 18 | CAN | 054 | 36 | 6 |
| 025 | 19 | EM | 055 | 37 | 7 |
| 026 | 1A | SUB | 056 | 38 | 8 |
| 027 | 1B | ESC | 057 | 39 | 9 |
| 028 | 1C | FS | 058 | 3A | : |
| 029 | 1D | GS | 059 | 3B | ; |

| Decimal | Hex | Character | Decimal | Hex | Character |
|---|---|---|---|---|---|
| 060 | 3C | < | 094 | 5E | ^ |
| 061 | 3D | = | 095 | 5F | — |
| 062 | 3E | > | 096 | 60 | ` |
| 063 | 3F | ? | 097 | 61 | a |
| 064 | 40 | @ | 098 | 62 | b |
| 065 | 41 | A | 099 | 63 | c |
| 066 | 42 | B | 100 | 64 | d |
| 067 | 43 | C | 101 | 65 | e |
| 068 | 44 | D | 102 | 66 | f |
| 069 | 45 | E | 103 | 67 | g |
| 070 | 46 | F | 104 | 68 | h |
| 071 | 47 | G | 105 | 69 | i |
| 072 | 48 | H | 106 | 6A | j |
| 073 | 49 | I | 107 | 6B | k |
| 074 | 4A | J | 108 | 6C | l |
| 075 | 4B | K | 109 | 6D | m |
| 076 | 4C | L | 110 | 6E | n |
| 077 | 4D | M | 111 | 6F | o |
| 078 | 4E | N | 112 | 70 | p |
| 079 | 4F | O | 113 | 71 | q |
| 080 | 50 | P | 114 | 72 | r |
| 081 | 51 | Q | 115 | 73 | s |
| 082 | 52 | R | 116 | 74 | t |
| 083 | 53 | S | 117 | 75 | u |
| 084 | 54 | T | 118 | 76 | v |
| 085 | 55 | U | 119 | 77 | w |
| 086 | 56 | V | 120 | 78 | x |
| 087 | 57 | W | 121 | 79 | y |
| 088 | 58 | X | 122 | 7A | z |
| 089 | 59 | Y | 123 | 7B | { |
| 090 | 5A | Z | 124 | 7C | \| |
| 091 | 5B | [ | 125 | 7D | } |
| 092 | 5C | \ | 126 | 7E | ~ |
| 093 | 5D | ] | 127 | 7F | DEL |

Notes: