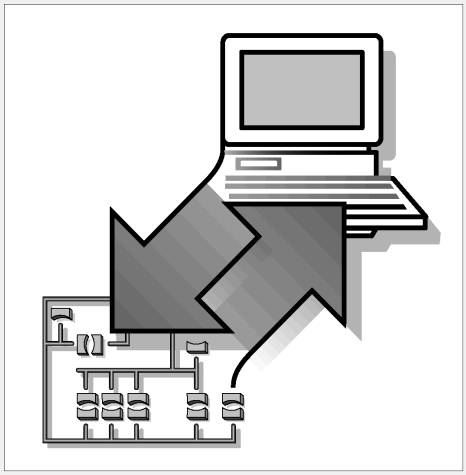
Allen-Bradley

1785 PLC-5® Programmable Controllers

Addressing Reference Manual



Important User Information

Because of the variety of uses for the products described in this publication, those responsible for the application and use of this control equipment must satisfy themselves that all necessary steps have been taken to assure that each application and use meets all performance and safety requirements, including any applicable laws, regulations, codes and standards.

The illustrations, charts, sample programs and layout examples shown in this guide are intended solely for purposes of example. Since there are many variables and requirements associated with any particular installation, Allen-Bradley does not not assume responsibility or liability (to include intellectual property liability) for actual use based upon the examples shown in this publication.

Allen-Bradley publication SGI–1.1, Safety Guidelines for the Application, Installation, and Maintenance of Solid-State Control (available from your local Allen-Bradley office), describes some important differences between solid-state equipment and electromechanical devices that should be taken into consideration when applying products such as those described in this publication.

Throughout this manual we use notes to make you aware of safety considerations.

ATTENTION: Identifies information about practices or circumstances that can lead to personal injury or death, property damage or economic loss.

Attention statements help you to:

- identify a hazard
- avoid the hazard
- recognize the consequences

Important: Identifies information that is critical for successful application and understanding of the product.

Summary of Changes

New Information

This release of the publication contains new and revised information. To help you find this information, we have included change bars as shown to the left of this paragraph.

For This Specific Revised Information	Refer to:
updated product and documentation references	throughout this manual
updated status file description	page 6

Addressing for 1785 PLC-5 Processors

Using this Addressing Reference Guide

This addressing reference guide helps you specify the address in a 1785 PLC-5® data table. This reference contains:

A 1785 PLC-5 processor may include the following processors:

- PLC-5/10™
- PLC-5/11™
- PLC-5/12™
- PLC-5/15™
- PLC-5/20™
- PLC-5/25™
- PLC-5/30™
- PLC-5/40™
- PLC-5/40L™
- PLC-5/60™
- PLC-5/60L™
- PLC-5/80™

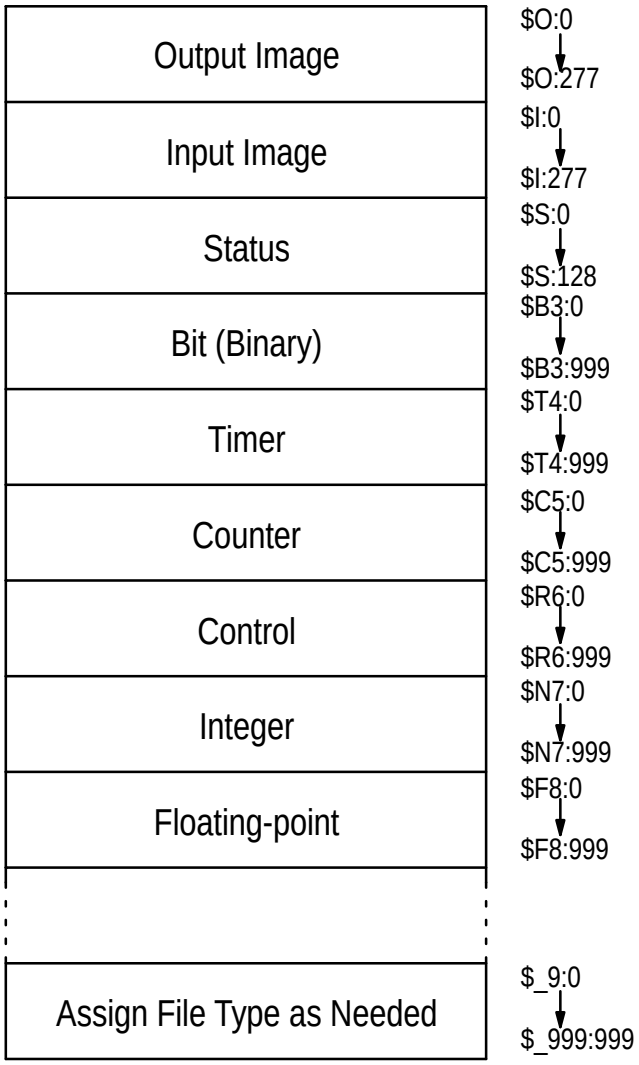
For more information about the specific contents of the various sections of memory, consult the:

- PLC® programmer, who assigns specific data items to specific memory locations
- PLC-5 Programming Software Configuration and Maintenance Manual, publication 6200–6.4.6

Memory Map

The memory map in Figure 1 shows the logical arrangement of the data table area of memory in a 1785 PLC-5 processor. This map does not represent the physical structure of the memory, but it provides the addressing scheme for the memory in the 1785 PLC-5 data table. The logical ASCII formats for the memory addresses you can access are shown in subsequent figures for each section.

Figure 1
Memory Map of 1785 PLC-5 Processors



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Locating Addressing Information

The remainder of this addressing reference provides addressing formats, mnemonics, and data structures for addressing various 1785 PLC-5 data–table sections. Use Table A to locate information about specific data types

Table A
Locating PLC-5 Addressing Information

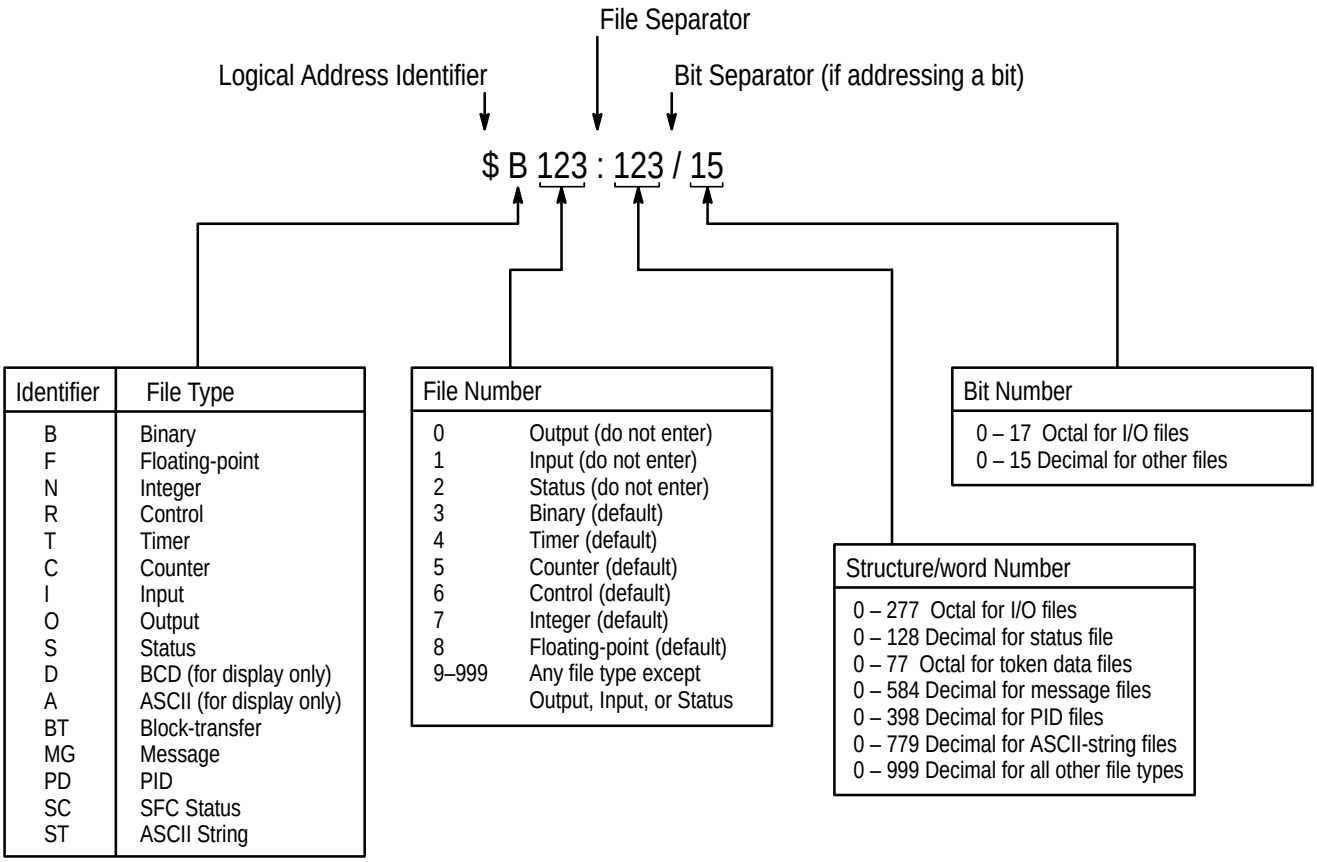
For Information About:	Refer to:
ASCII Data Files	Figure 7, Figure 8
ASCII String Files	Figure 13, Table M, Figure 19, Table N
BCD Data Files	Figure 7, Figure 10
Binary Files	Figure 7, Figure 9
Block-transfer Control Files	Figure 13, Table K, Figure 18, Table L
Control Files	Figure 13, Table G, Figure 16, Table H
Counter Files	Figure 13, Table E, Figure 15, Table F
Floating-point files	Figure 7, Figure 11
Input File	Figure 3, Figure 4
Integer Files	Figure 7, Figure 12
Message Control files	Figure 13, Table R, Figure 21, Table S
Output File	Figure 3, Figure 4
PID Control Files	Figure 13, Table O, Figure 20, Table P
SFC Status Files	Figure 13, Table I, Figure 17
Status File	Figure 5, Figure 6, Table B
Timer Files	Figure 13, Table C, Figure 14, Table D

Use logical ASCII addressing to read and write data to and from the PLC-5 data table. You provide a string of letters, digits, and punctuation that specifies the file type, file, and structure or word of the address.

General Format for Logical ASCII Addressing

Figure 2 illustrates the general format for logical addressing in the data table of the 1785 PLC-5 memory.

Figure 2
General Format for Logical Addressing



Note: BT, MG, PD, SC, and ST files are not available on PLC-5/10, -5/12, -5/15, and -5/25 processors. In addition, since the output, input, and status files are automatically assigned files numbers 0, 1, and 2 respectively, do not enter a file number for these files.

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Note that throughout this publication we use **$** as the logical address identifier. This is an entry for INTERCHANGE software. It is also an entry for 6200 software in sending a message from some other stations to a PLC-5 station. It is not used in 6200 software for internal addressing.

Figures 3 through 23 show specific formats for logical addressing of various areas of the 1785 PLC-5 data table.

Logical Addressing for I/O Image Tables

Figure 3
Logical Addressing for I/O Image Tables

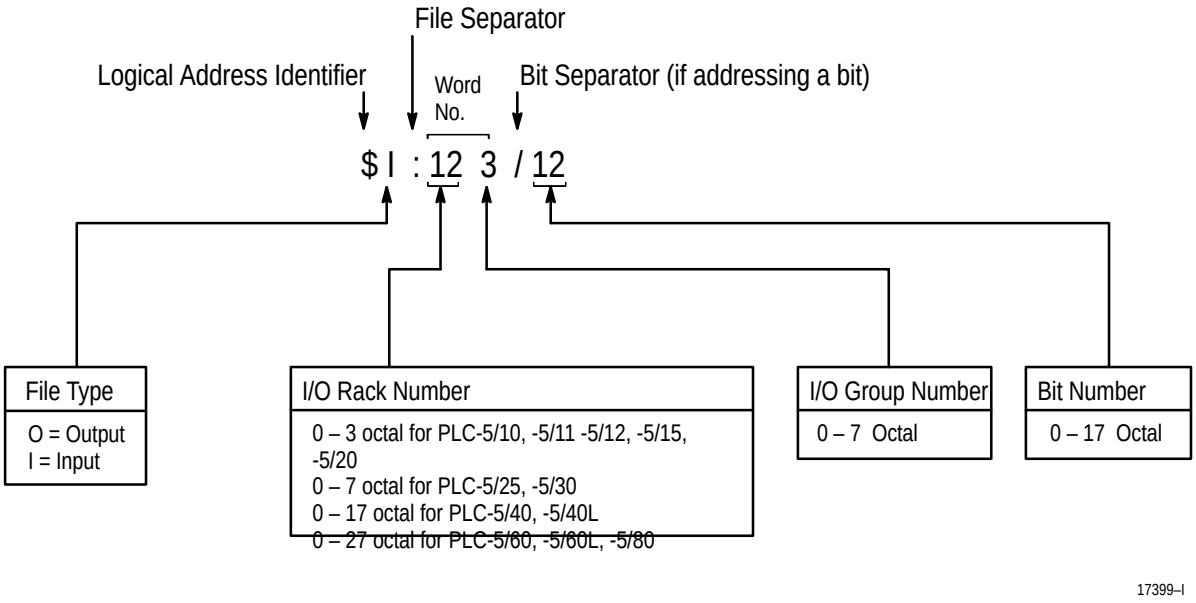

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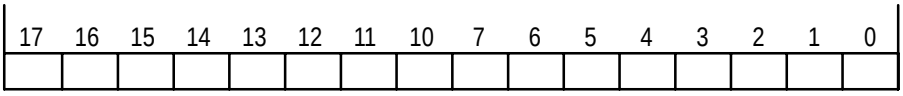
Figure 4
Word of Input or Output Image File



PLC Data Type: signed word (negative values in 2's complement form)
Range: –32,768 thru +32,767

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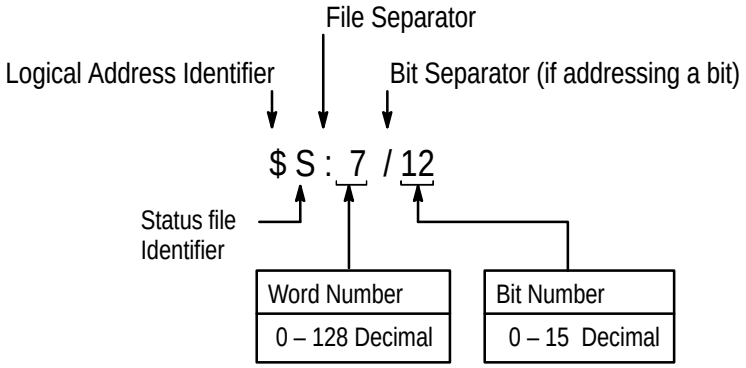
Logical Addressing for the Status File

Figure 5 shows how to address the status file of the PLC-5 data table. Figure 6 shows a word of the status file. Figure 5 shows what is stored in each word of the status file. For more information, refer to the PLC-5 Programming Software Configuration and Maintenance Manual, publication 6200-6.4.6.

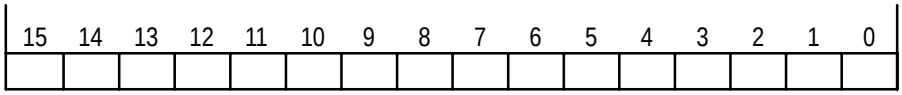
Figure 5
Logical Addressing for the Status File



Note: Word number is 0 – 31 on PLC-5/10, -5/12, -5/15, and -5/25 processors.

17401–I

Figure 6
Word of Status file



PLC Data Type: signed word (negative values in 2's complement form)
Range: –32,768 thru +32,767

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Table B
Status File Description

This word of the status file:	Stores:
S:0	Arithmetic flags • bit 0 = carry • bit 1 = overflow • bit 2 = zero • bit 3 = sign

This word of the status file:	Stores:
S:1	Processor status and flags Bit — Description 0 — RAM checksum is invalid at power-up 1 — processor in RUN mode 2 — processor in TEST mode 3 — processor in PROG mode 4 — processor burning EEPROM 5 — enabled download operation 6 — enabled test edit mode 7 — mode select switch in REMOTE position 8 — forces enabled 9 — forces present 10 — processor successfully burned EEPROM 11 — preforming online programming 12 — not defined 13 — user program checksum done 14 — last scan of ladder or SFC step 15 — processor started first program scan or the first scan of the next step in an SFC
S:2	Switch Setting information • bits 0 – 7 DH+ station number • bits 11–12 are set based on the I/O chassis backplane switches bit 12 — bit 11 = I/O chassis addressing 0 — 0 — illegal 1 — 0 — 1/2 -slot 0 — 1 — 1-slot 1 — 1 — 2-slot • bit 13: 1 = load from EEPROM • bit 14: 1 = RAM backup not configured • bit 15: 1 = memory unprotected
S:3 to S:6	Active Node table for channel 1A Word — Bits — DH+ Station # 3 — 0-15 — 00-17 4 — 0-15 — 20-37 5 — 0-15 — 40-57 6 — 0-15 — 60-77
S:7	Global status bits: • low 8 bits – rack fault bits for racks 0-7 • high 8 bits – rack queue-full bits for racks 0-7
S:8	Last program scan (in ms)
S:9	Maximum program scan (in ms)

This word of the status file:	Stores:
S:10	Minor fault (word 1) Bit — Description 0 — battery is low (replace in 1-2 days) 1 — DH+ table has changed (active node table) 2 — STI delay too short, interrupt program overlap 3 — EEPROM memory transfer at power-up 4 — edits prevent SFC continuing 5 — invalid I/O status file 6 — not defined 7 — no more command blocks exist 8 — not enough memory on the memory module to upload the program from the processor 9 — no MCP is configured to run 10 — MCP not allowed 11 — PII word number not in local rack 12 — PII overlap 13 — no command blocks exist to get PII 14 — arithmetic overflow 15 — SFC action overlap
S:11	Major fault Bit — Description 0 — corrupted program file (codes 10-19) 1 — corrupted address in ladder file (codes 10-29) 2 — programming error (codes 30-49) 3 — SFC fault (codes 71-79) 4 — error while assembling program (code 70) 5 — start-up protection fault) 6 — peripheral device fault 7 — jumped to fault routine (codes 0-9) 8 — watchdog faulted 9 — system configured wrong (codes 80-89) 10 — recoverable hardware error 11 — MCP does not exist or is not ladder or SFC file 12 — PII does not exist or is not ladder 13 — STI does not exist or is not ladder 14 — fault routine does not exist or is not ladder 15 — fault routine is not a ladder file

This word of the status file:	Stores:
S:12	Fault codes Code — Description 0-9 — user-defined 10 — failed data table check 11 — bad user program checksum 12 — bad integer operand type 13 — bad mixed mode operand type 14 — not enough operands for instruction 15 — too many operands for instruction 16 — bad instruction found 17 — no expression end 18 — missing end of edit zone 19 — download aborted 20 — indirect address out of range (high) 21 — indirect address out of range (low) 22 — attempt to access undefined file 23 — file number less than 0 or greater than the number of defined files: or, indirect reference to file 0, 1, 2; or bad file number 24 — indirect reference to wrong file type 30 — subroutine jump nesting level exceeded 31 — too few subroutine parameters 32 — jump to non-ladder file 33 — CAR routine not 68000 code 34 — bad timer parameters entered 35 — bad PID delta time entered 36 — PID setpoint out of range 37 — invalid I/O specified in an immediate I/O instruction 38 — invalid use of return instruction 39 — FOR loop missing NXT 40 — control file too small 41 — NXT instruction with no FOR 42 — jump target does not exist 43 — file is not an SFC 44 — error using SFR 45 — invalid channel number entered 46-69 — reserved
S:13	Program file where fault occurred
S:14	Rung number where fault occurred
S:15	VME status file
S:16	I/O status file

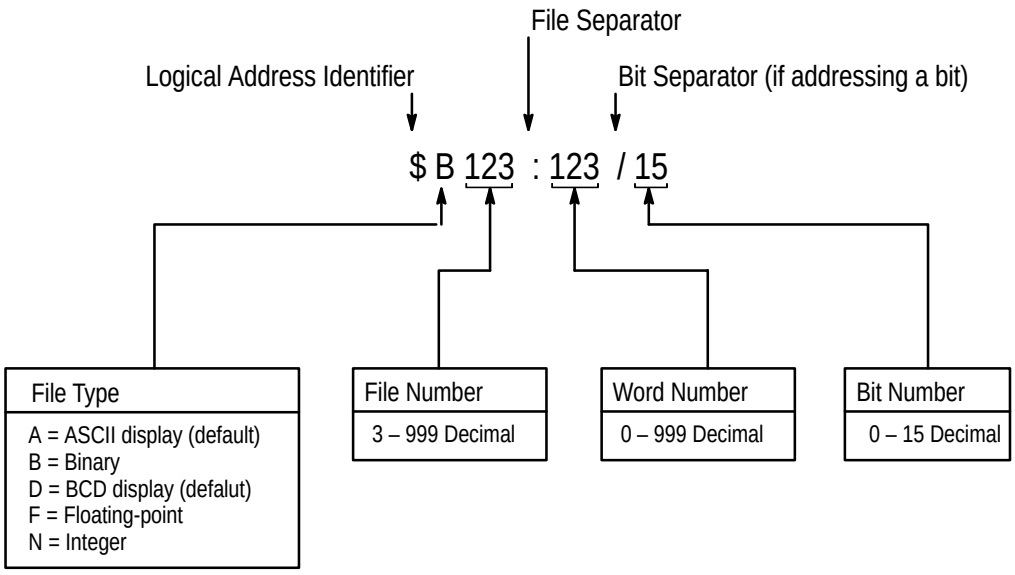
This word of the status file:	Stores:
S:17	Minor fault (word 2) Bit Description 0 BT queue full to remote I/O 1 queue full – channel 1A 2 queue full – channel 1B 3 queue full – channel 2A 4 queue full – channel 2B 5 no modem on serial port 6 remote I/O rack in local rack table; or, remote I/O rack is greater than the image size 8 ASCII instruction error 9 duplicate node address 10 DF1 master poll list error 11 protected processor data table element violation 12 protected processor file violation
S:18	Processor clock year
S:19	Processor clock month
S:20	Processor clock day
S:21	Processor clock hour
S:22	Processor clock minute
S:23	Processor clock second
S:24	Indexed addressing offset
S:26	User control bits Bit Description 0 Restart/continuous SFC: when reset, processor restarts at first step in SFC. When set, processor continues with active step after power loss or change to RUN. 1 Start-up protection after power loss; when reset, no protection. When set, processor executes fault routine at power-up (sets word 11, bit 5). 2 Define the address of the local rack: when reset, local rack address is 0. When set, local rack address is 1. 3 Set complementary I/O: when reset, complementary I/O is not enabled. When set, complementary I/O is enabled. 4 Local block transfer compatibility bit: when reset, normal operation. When set, eliminates frequent checksum errors to certain BT modules. 5 When set (1), delay adapter channel response by 1s for compatibility with PLC-3 scanners. When reset (0), operate in normal response time.
S:27	Rack control bits: • low 8 bits – I/O rack inhibit bits for racks 0-7 • high 8 bits – I/O rack reset bits for racks 0-7

This word of the status file:	Stores:
S:28	Program watchdog setpoint
S:29	Fault routine file
S:30	STI setpoint
S:31	STI file number
S:32	Global status bits: • low 8 bits – rack fault bits for racks 10-17 (octal) • high 8 bits – rack queue-full bits for racks 10-17
S:33	Rack control bits: • low 8 bits – I/O rack inhibit bits for racks 10-17 • high 8 bits – I/O rack reset bits for racks 10-17
S:34	Global status bits: • low 8 bits – rack fault bits for racks 20-27 (octal) • high 8 bits – rack queue-full bits for racks 20-27
S:35	Rack control bits: • low 8 bits – I/O rack inhibit bits for racks 20-27 • high 8 bits – I/O rack reset bits for racks 20-27
S:46	PII program file number
S:47	PII module group
S:48	PII bit mask
S:49	PII compare value
S:50	PII down count
S:51	PII changed bit
S:52	PII events since last interrupt
S:53	STI scan time (in ms)
S:54	STI maximum scan time (in ms)
S:55	PII last scan time (in ms)
S:56	PII maximum scan time (in ms)
S:57	User program checksum
S:59	Extended-local I/O channel discrete transfer scan (in ms)
S:60	Extended-local I/O channel discrete maximum scan (in ms)
S:62	Extended-I/O channel maximum block-transfer scan (in ms)
S:63	Protected processor data table protection file number

This word of the status file:	Stores:
S:77	Communication time slice for communication housekeeping functions (in ms)
S:78	MCP I/O update disable bits Bit 0 for MCP A Bit 1 for MCP B etc.
S:79	MCP inhibit bits Bit 0 for MCP A Bit 1 for MCP B etc.
S:80-S:127	MCP file number MCP scan time (in ms) MCP max scan time (in ms) The above sequence applies to each MCP; therefore, each MCP has 3 status words. For example, word 80: file number for MCP A word 81: scan time for MCP A word 82: maximum scan time for MCP A word 83: file number for MCP B word 84: scan time for MCP B etc.

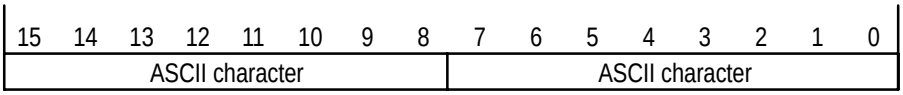
Logical Addressing for ASCII, Binary, BCD, Floating-Point, and Integer Files

Figure 7
Format for Logical Addressing of ASCII, Binary, BCD, Floating-Point, and Integer Files



Note: Except for data entry and display, all values in A, B, D, and N files are processed as integer values stored in natural binary format.

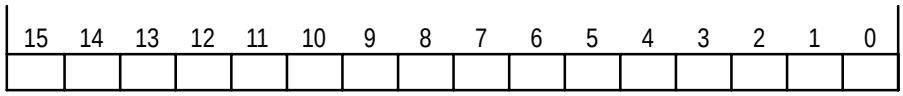
Figure 8
Word of ASCII (ANSI X3.4) File



PLC Data Type: signed word

17410–I

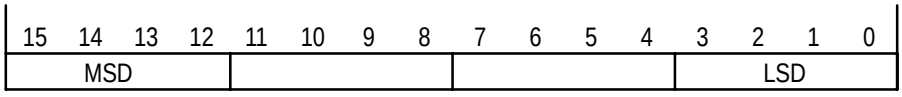
Figure 9
Word of a Binary File



PLC Data Type: signed word (negative values in 2's complement form)
Range: –32,768 thru +32,767

17411–I

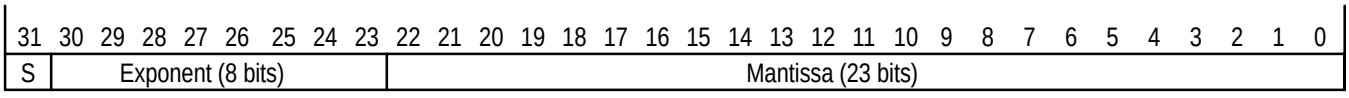
Figure 10
Word of Decimal (BCD) File



MSD = Most significant digit
LSD = Least Significant Digit
PLC Data Type: signed word
Display: BCD (4 digits per word) 0 thru 9,000

17412–I

Figure 11
Word of Floating-Point File



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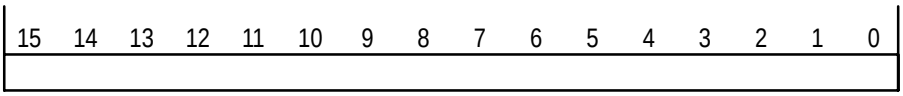
PLC Data Type: IEEE Float (32-bit value)
Range: +/– 1.1754944 E–38 thru +/– 3.4028237 E+38

Figure 12
Word of Integer File



PLC Data Type: signed word (negative values in 2's complement form)
Range: –32,768 thru +32,767

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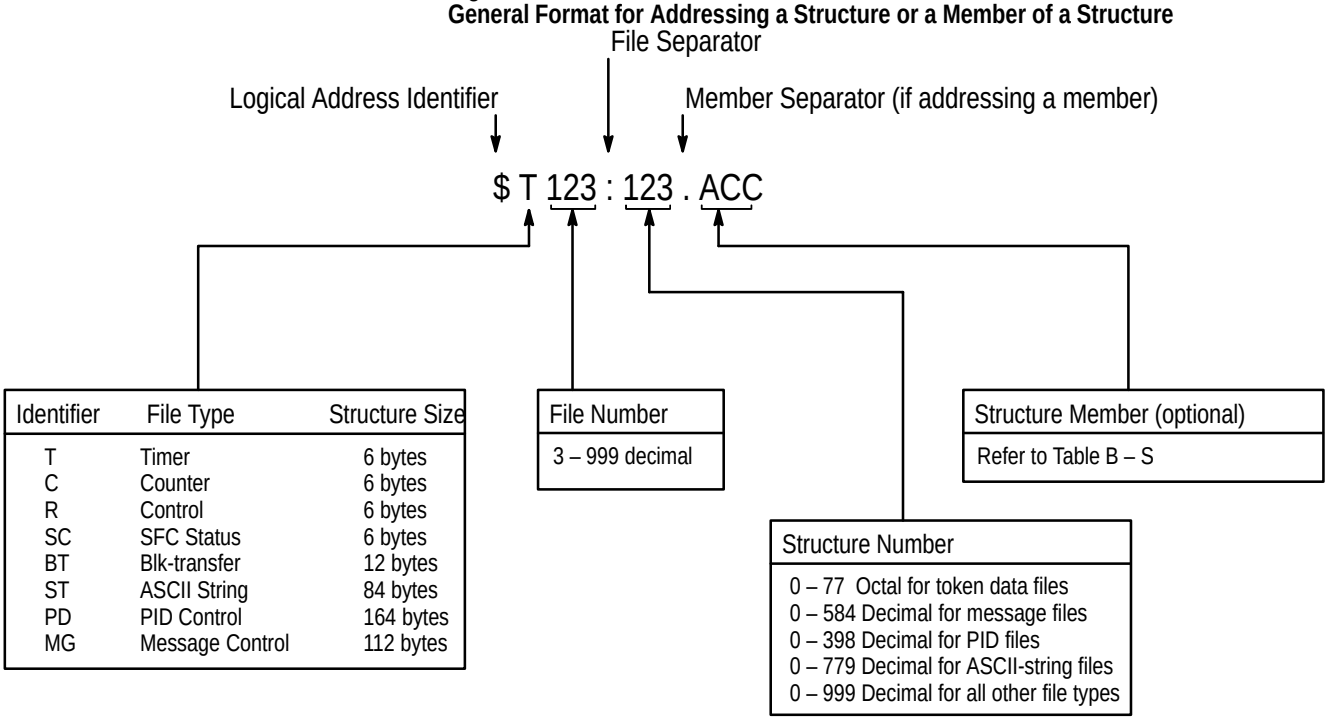
Addressing Structured Data

Figure 13 shows address formats for structured data. Figures 15 thru 22 and tables B thru L show data structures and mnemonics for the various file types.

Figure 13
General Format for Addressing a Structure or a Member of a Structure



Note: BT, MG, PD, SC, and ST files are not available on PLC-5/10, -5/12, -5/15, and -5/25 processors.

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Table C
Timer Mnemonics

Mnemonic	Structure Member	Size	PLC Data Type
.EN	Enable	1 bit	bit
.TT	Timing	1 bit	bit
.DN	Done	1 bit	bit
.PRE	Preset Value	2 bytes	signed word
.ACC	Accumulated Value	2 bytes	signed word

Figure 14
Timer Structure

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	TT	TD	Reserved					Used to maintain timer accuracy							
PRE – Preset Value (–32,768 thru +32,767)															
ACC – Accumulated Value (–32,768 thru +32,767)															

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Table D
Example Timer Addresses

To Address:	PLC Data Type:	Example Address:
Whole Timer Structure	structure	$T4:5
Timer Accumulated Word	signed word	$T4:3.ACC
Timer Preset Word	signed word	$T4:3.PRE
Timer Enabled Bit	bit	$T4:3.TE
Timer Timing Bit	bit	$T4:3.TT
Timer Done Bit	bit	$T4:3.TD

Table E
Counter Mnemonics

Mnemonic	Structure Member	Size	PLC Data Type
.CU	Up Enable	1 bit	bit
.CD	Down Enable	1 bit	bit
.DN	Done	1 bit	bit
.OV	Overflow	1 bit	bit
.UN	Underflow	1 bit	bit
.PRE	Preset Value	2 bytes	signed word
.ACC	Accumulated Value	2 bytes	signed word

Figure 15
Counter Structure

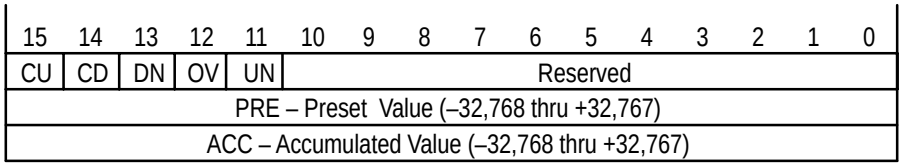

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Table F
Example Counter Addresses

To Address:	PLC Data Type:	Example Address:
Whole Counter Structure	structure	$C5:4
Counter Accumulated Word	signed word	$C5:7.ACC
Counter Preset Word	signed word	$C5:7.PRE
Counter Up Bit	bit	$C5:7.CU
Counter Down Bit	bit	$C5:7.CD
Counter Done Bit	bit	$C5:7.DN
Counter Overflow Bit	bit	$C5:7.OV
Counter Underflow Bit	bit	$C5:7.UN

Table G
Control Mnemonics

Mnemonic	Structure Member	Size	PLC Data Type
.EN	Enable	1 bit	bit
.EU	Enable Unloading	1 bit	bit
.DN	Done	1 bit	bit
.EM	Empty	1 bit	bit
.ER	Error	1 bit	bit
.UL	Unload	1 bit	bit
.IN	Inhibit Comparison	1 bit	bit
.FD	Found	1 bit	bit
.UL	Unload	1 bit	bit
.IN	Inhibit Comparisons	1 bit	bit
.LEN	Length	2 bytes	signed word
.POS	Position	2 bytes	signed word

Figure 16
Control Structure

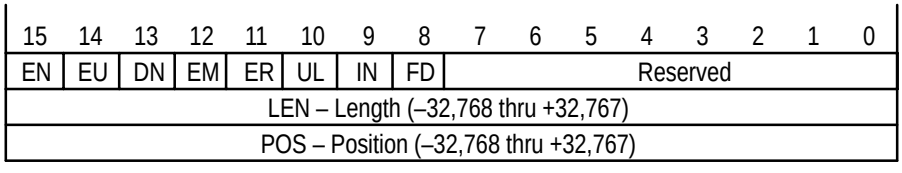

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Table H
Example Control Addresses

To Address:	PLC Data Type:	Example Address:
Whole Control Structure	structure	$R6:0
Control Position Word	signed word	$R6:0.POS
Control Length Word	signed word	$R6:0.LEN
Control Enable Bit	bit	$2R6:0.EN
Control Unload Enable Bit	bit	$2R6:0.EU
Control Done Bit	bit	$2R6:0.DN
Control Empty Bit	bit	$2R6:0.EM
Control Error Bit	bit	$2R6:0.ER
Control Unload Bit	bit	$2R6:0.UL
Control Inhibit Bit	bit	$2R6:0.IN
Control Found Bit	bit	$2R6:0.FD

Table I
SFC Status Mnemonics

Mnemonic	Structure Member	Size	PLC Data Type
.SA	Scan Active	1 bit	bit
.FS	First Scan	1 bit	bit
.LS	Last Scan	1 bit	bit
.OV	Timer Overflow	1 bit	bit
.ER	Step Errored	1 bit	bit
.DN	Done	1 bit	bit
.PRE	Preset Value	2 bytes	signed word
.TIM	Active Time	2 bytes	signed word

Figure 17
SFC Status Structure

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SA	FS	LS	OV	ER	DN	Reserved									
PRE – Preset Value (–32,768 thru +32,767)															
TIM – Active Time (–32,768 thru +32,767)															

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Table J
Example SFC Status Addresses

To Address:	PLC Data Type:	Example Address:
Whole SFC Status Structure	structure	$SC9:0
Preset Word	signed word	$SC9:0.PRE
Active-Time Word	signed word	$SC9:0.TIM
Scan-active Bit	bit	$SC9:0.SA
First-scan Bit	bit	$SC9:0.FS
Last-scan Bit	bit	$SC9:0.LS
Timer-overflow Bit	bit	$SC9:0.OV
Step-errored Bit	bit	$SC9:0.ER
Done Bit	bit	$SC9:0.DN

Table K
Block-Transfer Control Mnemonics

Mnemonic	Structure Member	Size	PLC Data Type
.EN	Enable	1 bit	bit
.ST	Start	1 bit	bit
.DN	Done	1 bit	bit
.ER	Error	1 bit	bit
.CO	Continue	1 bit	bit
.EW	Enabled Waiting	1 bit	bit
.NR	No Response	1 bit	bit
.TO	Time Out	1 bit	bit
.RW	Read/Write	1 bit	bit
.RLEN	Requested Word Count	2 bytes	signed word
.DLEN	Transmitted Word Count	2 bytes	signed word
.FILE	File-type Number	2 bytes	signed word
.ELEM	Word Number	2 bytes	signed word
.RGS	Rack/Group/Slot	2 bytes	signed word

Figure 18
Block-transfer Control Structure

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	ST	DN	ER	CO	EW	NR	TO	RW	Reserved						
RLEN – Requested Word Count (–32,768 thru +32,767)															
DLEN – Transmitted Word Count (–32,768 thru +32,767)															
FILE – File-type Number (–32,768 thru +32,767)															
ELEM – Word Number (–32,768 thru +32,767)															
I/O Rack											not used	I/O Group			slot

Table L
Example Block-transfer Control Addresses

To Address:	PLC Data Type:	Example Address:
Whole B-T Control Structure	structure	$BT10:0
Requested-word Count	signed word	$BT10:0.RLEN
Transmitted-word Count	signed word	$BT10:0.DLEN
File-type Number	signed word	$BT10:0.FILE
Word Number	signed word	$BT10:0.ELEM
Rack/Group/Slot	signed word	$BT10:0.RGS
Done Bit	bit	$BT10:0.DN

Table M
ASCII String Mnemonics

Mnemonic	Structure Member	Size	PLC Data Type
.LEN	Length	2 bytes	signed word

Figure 19
ASCII String Structure

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEN – Length specifies an even number of bytes (2 – 82)															
A maximum of 82 bytes of data accessible only by addressing the whole structure.															

Table N
Example ASCII Structure Addresses

To Address:	PLC Data Type:	Example Address:
Whole ASCII String Structure	structure	$ST12:0
Length Word	signed word	$ST12:0.LEN

Table O
PID Mnemonics in PD File

Mnemonic	Structure Member	Size	PLC Data Type
.INI	PID Initialized	1 bit	bit
.SPOR	SP Out of Range	1 bit	bit
.OLL	Output Limit Low	1 bit	bit
.OLH	Output Limit High	1 bit	bit
.EWD	Error Within Dead Band	1 bit	bit
.DVNA	Deviation High Alarm	1 bit	bit
.DVPA	Deviation Low Alarm	1 bit	bit
.PVLA	PV Low Alarm	1 bit	bit
.PVHA	PV High Alarm	1 bit	bit
.EN	Enable	1 bit	bit
.CT	Cascaded Type	1 bit	bit
.CL	Cascaded Loop	1 bit	bit
.PVT	PV Tracking	1 bit	bit
.DO	Derivative	1 bit	bit
.SWM	Software A/M Mode	1 bit	bit
.CA	Control Action	1 bit	bit
.MO	Station Mode (auto/manual)	1 bit	bit
.PE	PID Equation Type	1 bit	bit
.SP	Set Point	4 bytes	IEEE float
.KP	Proportional Gain	4 bytes	IEEE float
.KI	Integral Gain	4 bytes	IEEE float
.KD	Derivative Time	4 bytes	IEEE float
.BIAS	Output Bias %	4 bytes	IEEE float
.MAXS	Set–point Maximum (scaled value)	4 bytes	IEEE float
.MINS	Set–point Minimum (scaled value)	4 bytes	IEEE float
.DB	Dead Band	4 bytes	IEEE float
.SO	Set Output %	4 bytes	IEEE float
.MAXO	Output Limit High %	4 bytes	IEEE float
.MINO	Output Limit Low %	4 bytes	IEEE float
.UPD	Update Time	4 bytes	IEEE float
.PV	Process Variable	4 bytes	IEEE float
.ERR	Error	4 bytes	IEEE float
.OUT	Output %	4 bytes	IEEE float
.PVH	PV Alarm High	4 bytes	IEEE float
.PVL	PV Alarm Low	4 bytes	IEEE float
.DVP	Deviation Alarm +	4 bytes	IEEE float
.DVN	Deviation Alarm –	4 bytes	IEEE float
.PVDB	PV Alarm Dead Band	4 bytes	IEEE float

Mnemonic	Structure Member	Size	PLC Data Type
.DVDB	Deviation Alarm Dead Band	4 bytes	IEEE float
.MAXI	Input Range Maximum	4 bytes	IEEE float
.MINI	Input Range Minimum	4 bytes	IEEE float
.TIE	Tieback %	4 bytes	IEEE float
.ADDR[1]	Address of Master for the Slave	4 X 2 bytes	signed words
.DATA[2]	Reserved/Internal Use	14 X 4 bytes	IEEE float

[1] 0 – 3 [2] 0 – 13

Figure 20
PID Control Structure in PD file

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN						CT	CL	PVT	DO		SWM		CA	MO	PE
			INI	SPOR	OLL	OLH	EWD					DVNA	DVPA	PVLA	PVHA

SP	Set Point	4 bytes	IEEE float
KP	Proportional Gain	4 bytes	IEEE float
KI	Initial Gain	4 bytes	IEEE float
KD	Derivative Gain	4 bytes	IEEE float
BIAS	Output Bias %	4 bytes	IEEE float
MAXS	Maximum Scaled Value	4 bytes	IEEE float
MINS	Minimum Scaled Value	4 bytes	IEEE float
DB	Dead Band	4 bytes	IEEE float
SO	Set Output %	4 bytes	IEEE float
MAXO	Maximum Output Limit	4 bytes	IEEE float
MINO	Minimum Output Limit	4 bytes	IEEE float
UPD	Update Time	4 bytes	IEEE float
PV	Process Variable	4 bytes	IEEE float
ERR	Error: Scaled	4 bytes	IEEE float
OUT	Output	4 bytes	IEEE float
PVH	PV Alarm High	4 bytes	IEEE float
PVL	PV Alarm Low	4 bytes	IEEE float
DVP	Deviation Alarm +	4 bytes	IEEE float
DVN	Deviation Alarm –	4 bytes	IEEE float
PVDB	PV Alarm Dead Band	4 bytes	IEEE float
DVDB	Deviation Alarm Dead Band	4 bytes	IEEE float
MAXI	Maximum Input	4 bytes	IEEE float
MINI	Minimum Input	4 bytes	IEEE float
TIE	Tieback %	4 bytes	IEEE float
ADDR [0] thru ADDR [3]	Master-to-Slave Address	8 bytes	signed words
DATA [0] thru DATA [13]	Reserved / Internal Use	14 X 4 bytes	IEEE float

Table P
Example PID Control Addresses

To Address:	PLC Data Type:	Example Address:
Whole PD Control Structure	structure	$PD13:0
Set-point value	IEEE float	$PD13:0.SP
Proportional-gain value	IEEE float	$PD13:0.KP
PID-initialized bit	bit	$PD13:0.INI
SP out-of-range bit	bit	$PD13:0.SPOR

Table Q
PID Control Block in Integer File

Word:	Contains:		Term:	Range:
0	Bit 15 Enabled (EN) Bit 13 Done (DN) Bit 11 Set point out of range Bit 10 Output alarm, lower limit Bit 9 Output alarm, upper limit Bit 8 DB, set when error is in DB Bit 7 Resume last state (0 = yes, 1 = hold last state) Bit 6 Derivative action (0 = PV, 1 = error) Bit 5 Setpoint descaling (0 = no, 1 = yes) Bit 4 Set output (0 = no, 1 = yes) Bit 3 Output limiting ((0 = no, 1 = yes) Bit 2 Control (0 = direct, 1 = reverse) Bit 1 Mode (0 = automatic, 1 = manual) Bit 0 Equation (0 = independent, 1 = ISA)			
1	reserved			
2	Setpoint		SP	0 thru 4095 (unscaled) S_{min} thru S_{max} (scaled)
3	**Independent:**	Proportional gain (unitless)	K_P	0 thru 327.67
	ISA:	Controller gain (unitless)	K_C	0 thru 327.67
4	**Independent:**	Integral gain (1/s)	K_I	0 thru 327.67
	ISA:	Reset term (minutes per repeat)	T_I	0 thru 327.67
5	**Independent:**	Derivative gain	K_D	0 thru 327.67
	ISA:	Rate term x 100 (minutes)	T_D	0 thru 327.67
6	Feedforward or bias		FF/Bias	0 thru 4095
7	Maximum scaling		S_{max}	–32,768 thru +32,767
8	Minimum scaling		S_{min}	–32,768 thru +32,767
9	Dead band		DB	0 thru 4095 (unscaled) S_{min} thru S_{max} (scaled)
10	Set output		SETOUT	0 thru 100%
11	Maximum output limit (% of output)		L_{max}	0 thru 100%
12	Minimum output limit (% of output)		L_{min}	0 thru 100%
13	Loop update time (seconds)		dt	0.01 thru 327.67

Word:	Contains:	Term:	Range:
14	Scaled PV value (displayed)		S_{min} thru S_{max}
15	Scaled error value (displayed)		S_{min} thru S_{max}
16	Output (% of 4095)	CV	0 thru 100%
17 – 22	internal storage; do not use		

Table R
Message control Mnemonics in MG File

Mnemonic	Structure Member	Size	PLC Data Type
.NR	No Response	1 bit	bit
.TO	Time Out	1 bit	bit
.EN	Enable	1 bit	bit
.ST	Start Transmission	1 bit	bit
.DN	Done	1 bit	bit
.ER	Error	1 bit	bit
.CO	Continuous	1 bit	bit
.EW	Enabled Waiting	1 bit	bit
.ERR	Error Code	2 Bytes	signed word
.RLEN	Request Length	2 Bytes	signed word
.DLEN	Done Length	2 Bytes	signed word
.DATA[0] thru .DATA[51]	Reserved / Internal Use	52 X 2 Bytes	signed word

Figure 21
Message Control Structure in MG File

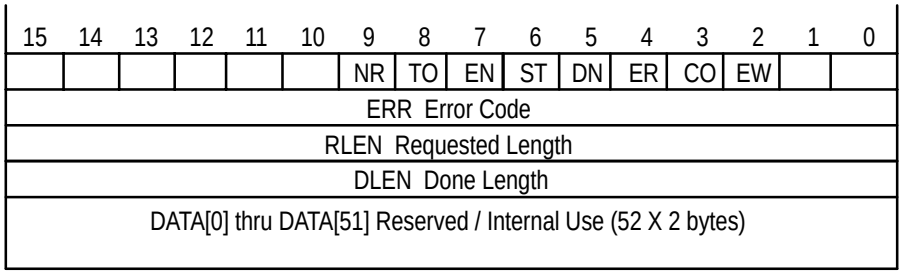
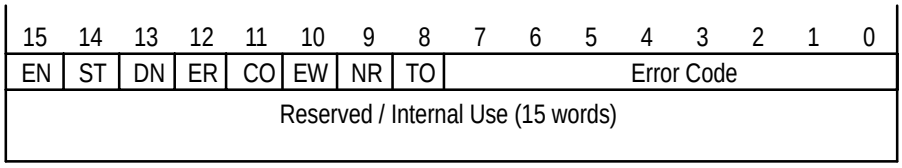


Table S
Example Message Control Addresses

To Address:	PLC Data Type:	Example Address:
Whole Message Control Structure	structure	$MG14:0
Request Length	signed word	$MG14:0.RLEN
Done bit	bit	$MG14:0.DN

Figure 22
Message Control Block in Integer File



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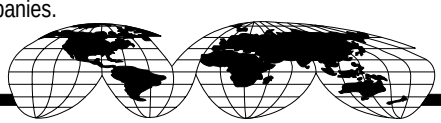

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